

ARTESYN DS760SL SERIES

760 Watts Distributed Power System



PRODUCT DESCRIPTION

Advanced Energy's Artesyn DS760SL series bulk front end AC-DC power supply accepts a wide range 90 to 264Vac input and provides a main 12V output plus a 5V standby output. Rated at 760 watts it has a high peak efficiency of 91%. Housed in a slimline 1U high, 2.1 in wide rack-mounting package, the power supply is primarily designed for 'always-on' enterprise servers and similar space-constrained applications. This series comes in two airflow versions — dc-connector to ac-connector and vice versa.

AT A GLANCE

Total Power:

760 Watts

Input Voltage:

90 to 264 Vac

of Outputs:

Main and Standby

SPECIAL FEATURES

- 1U × 54.5mm form factor (slimline) (5V standby - consult factory)
- 760W output power
- Active power factor correction
- N+1 redundant
- 18.1W/in³
- Internal OR'Ing
- 5.0V housekeeping
- Hot-swap
- High efficiency 91% @ 230Vac, 50% load
- Variable speed "smart fans"
- EMI Class A
- EN61000 Immunity
- Two years warranty

SAFETY

- UL/cUL 60950-1
- CSA 60950-1
- VDE 60950-1
- China CCC
- CB Scheme Report/Cert
- BSMI

TYPICAL APPLICATIONS

■ Industrial



MODEL NUMBERS

Standard	Output Voltage	Minimum Load	Maximum Load	Stand-By Supply	Air Flow Direction
DS760SL-3	12.0Vdc	0A	62.3A	5.0V@2.4A	Standard (DC Connector to Handle)
DS760SL-3-001	12.0Vdc	0A	50.0A	5.0V@2.4A	Reverse (Handle to DC Connector)
DS760SL-3-002	12.0Vdc	0A	62.3A	3.3V@2.4A	Standard (DC Connector to Handle)
DS760SL-3-003	12.0Vdc	0A	50.0A	3.3V@2.4A	Reverse (Handle to DC Connector)

Options

None



Absolute Maximum Ratings

Stress in excess of those listed in the "Absolute Maximum Ratings" may cause permanent damage to the power supply. These are stress ratings only and functional operation of the unit is not implied at these or any other conditions above those given in the operational sections of this TRN. Exposure to any absolute maximum rated condition for extended periods may adversely affect the power supply's reliability.

Table 1. Absolute Maximum Ratings								
Parameter	Models	Models Symbol		Тур	Max	Unit		
Input Voltage AC continuous operation	All models	V _{IN,AC}	90	-	264	Vac		
Maximum Output Power (Main + Stand-by)	DS760SL-3 DS760SL-3-001 DS760SL-3-002 DS760SL-3-003	P _{O,max}	- - - -	- - - -	760 600 760 600	W W W		
Isolation Voltage Input to outputs Input to safety ground	All models All models			- -	2121 2121	Vac Vdc		
Ambient Operating Temperature	All models	T _A	-10	-	50	°C		
Storage Temperature	All models	T _{STG}	-40	-	85	°C		
Humidity (non-condensing) Operating Non-operating	All models All models		7 5	-	93 95	% %		
Altitude Operating Non-operating	All models All models			-	4000 13000	m m		



Input Specifications

Table 2. Input Specifications						
Parameter	Condition	Symbol	Min	Тур	Max	Unit
Operating Input Voltage, AC		V _{IN,AC}	90	115/230	264	Vac
Input Vac Source Frequency		f _{IN,AC}	47	50/60	63	Hz
Maximum Input Current $(I_O = I_{O,max}, I_{SB} = I_{SB,Max})$	V _{IN,AC} = 100Vac	I _{IN} "max	ı	-	9	А
Standby Input Current $(V_O \text{ Off, } I_{SB} = 0A)$	V _{IN,AC} = 90Vac V _{IN,AC} = 180Vac	I _{I,standby}	-	-	400 300	mA mA
No Load Input Current $(V_O On, I_O = 0A, I_{VSB} = 0A)$	V _{IN,AC} = 90Vac V _{IN,AC} = 180Vac	I _{I,no_load}	-	-	800 450	mA mA
Harmonic Line Currents	All THD		Per IEC61000-3-2			
Power Factor	All		-	0.99	-	
Startup Surge Current (Inrush) @ 25°C	V _{IN,AC} = 264Vac		-	-	25	А
Input Fuse	Internal, L and N 5x20mm, Quick Acting 10A, 250V		-	-	10	А
Leakage Current to earth ground	V _{IN,AC} = 264Vac f _{IN,AC} = 50/60Hz		-	-	1.5	mA
Operating Efficiency @ 25°C	$I_{O} = I_{O,max}$ $V_{IN,AC} = 100Vac$ $V_{IN,AC} = 230Vac$	η	87 87	-	-	%
System Stability Phase Margin Gain Margin			45 6	-	-	Ø dB



Output Specifications

Table 3. Output Specif	fications						
Parameter		Condition	Symbol	Min	Тур	Max	Unit
Output Regulation	All models	Inclusive of set-point, temperature change,	V _O	11.88	12.0	12.12	V
Output Regulation	All Hodels	warm-up drift and dynamic load	V _{SB}	4.75	5.0	5.25	V
Output Ripple, pk-pk	All models	Measure with a 0.1uF ceramic capacitor in parallel with a 10uF	V _O	ı	-	100	mV _{PK-PK}
Output hippie, pk-pk	All Models	tantalum capacitor, 0 to 20MHz bandwidth.	V _{SB}	-	-	100	mV _{PK-PK}
Output Current	DS760SL-3 DS760SL-3-001 DS760SL-3-002	90Vac ≤ V _{IN,AC} ≤ 264Vac	Io	0 0 0	- - - -	62.3 49.0 63.3 49.0	А
	DS760SL-3-003		I _{SB}	0	-	2.4	А
V _O Current Share Accura	acy ¹	20% to 100% l ₀ ≤ 20% l ₀		-		10 3.11	%l _o A
V _O Minimum Load for Cu	urrent Sharing			20	-	-	%I _{O,max}
V _O Load Capacitance		Start up		-	5000	30000	uF
V _{SB} Load Capacitance		Start up		-	3000	10000	uF
V _O Dynamic Response Peak Deviation Settling Time		50% load change, slew rate = 1A/ms	±%V _o T _s	-		1 250	% uSec
V _O Long Term Stability Max change over 24 hou	ırs	After thermal equilibrium (30 mins)	±%V _O	-	-	0.2	%

Note 1 - This is typical testing results of two sample, it does not representing the extreme cases (one unit set to +0.5% above and one unit set to -0.5% below nominal).

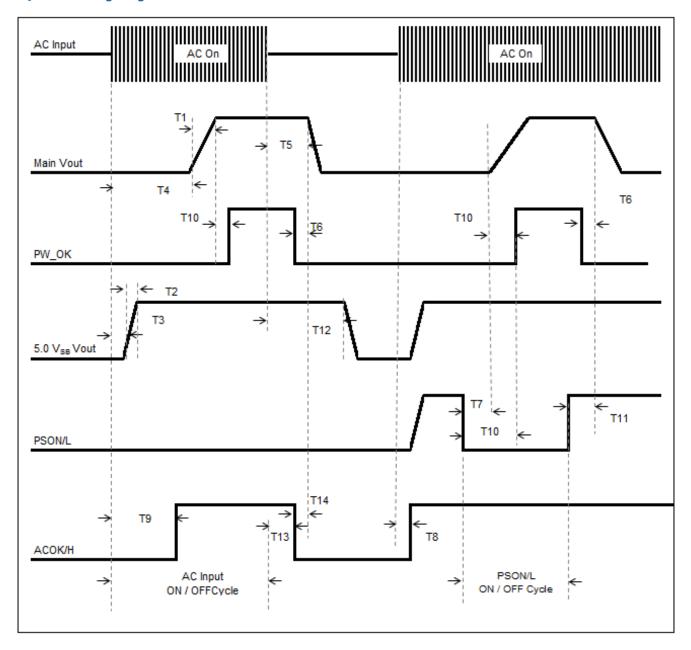


System Timing Specifications

Table 4.	ble 4. System Timing Specifications							
Label	Parameter	Min	Тур	Max	Unit			
T1	+12V output rise time	10	-	300	mSec			
T2	5.0Vsb output rise time	10	-	300	mSec			
ТЗ	Delay from AC being applied to 5.0Vsb begin to rise up	-	-	1500	mSec			
T4	Delay from AC being applied to 12Vdc begin to rise up	-	-	3000	mSec			
T5	T5 Time all 12Vdc hold up time after loss of AC		-	-	mSec			
Т6	Delay from loss of 12Vdc to de-assertion of PW_OK	-1	-	1	mSec			
T7	Delay from PSON/L active to output voltages starts rise up	45	-	2500	mSec			
T8	Delay ACOK/H after AC recycle	0	-	300	mSec			
Т9	Delay from sense of AC input to de-assertion of ACOK/H	0	-	600	mSec			
T10	Delay PSON/L to PW_OK asserted at turn on	100	-	500	mSec			
T11	Delay from PSON/H to 12Vdc dropping out of regulation limits	0	-	100	mSec			
T12	Duration of 5.0Vsb hold up after loss of AC		-	-	mSec			
T13	ACOK/L detected after loss of AC		-	-	mSec			
T14	Warn of AC loss before 12Vdc drop out of regulation		-	-	mSec			

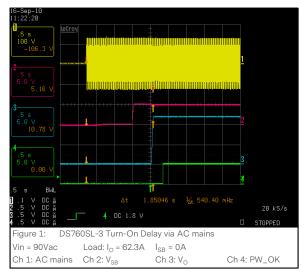


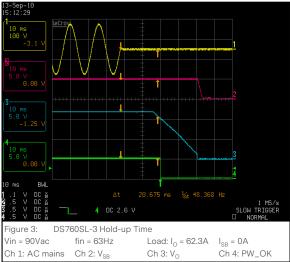
System Timing Diagram

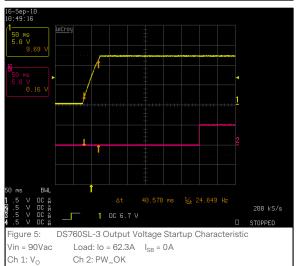


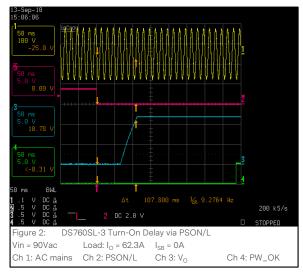


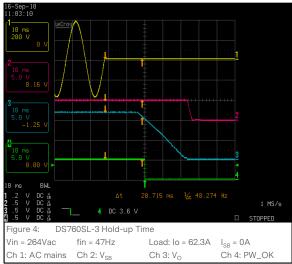
DS760SL-3 Performance Curves

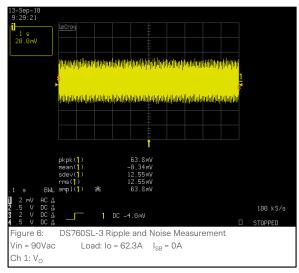






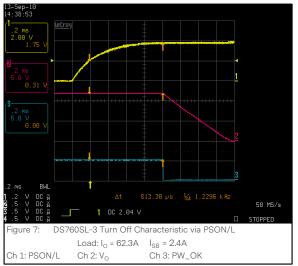


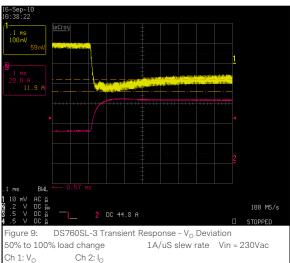


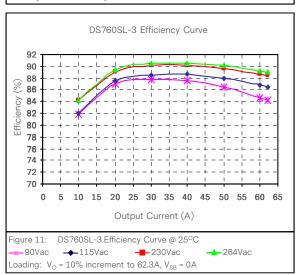


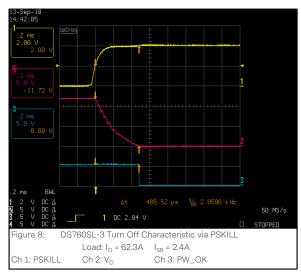


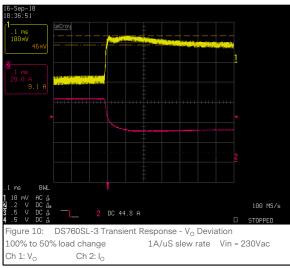
DS760SL-3 Performance Curves





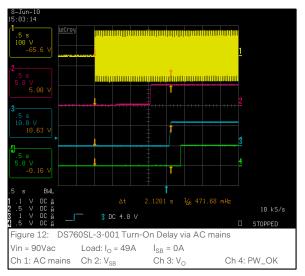


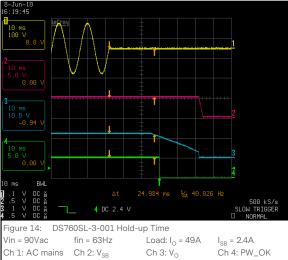


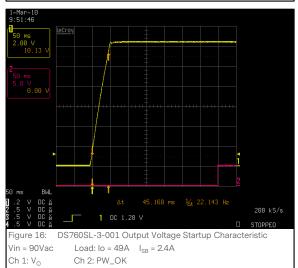


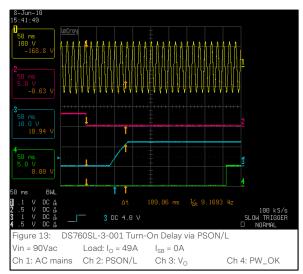


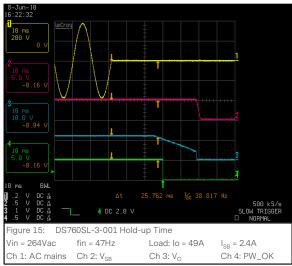
DS760SL-3-001 Performance Curves

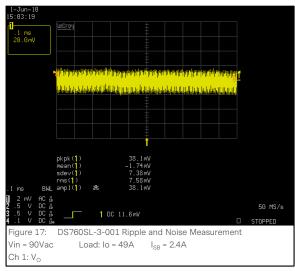








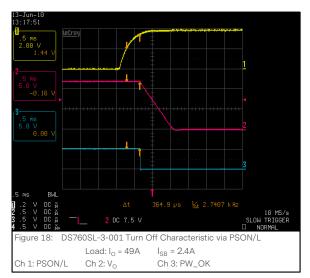


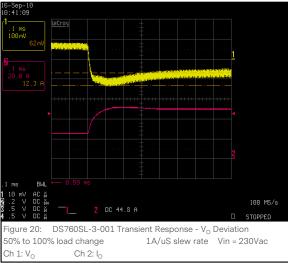


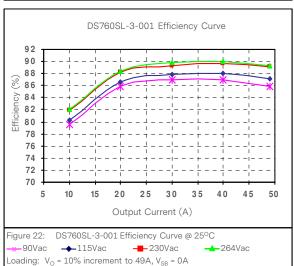


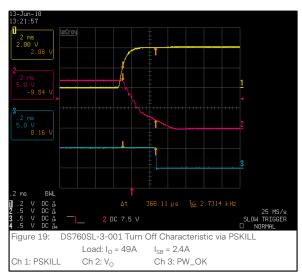
Rev. 03.03.21_#1.5 advancedenergy.com

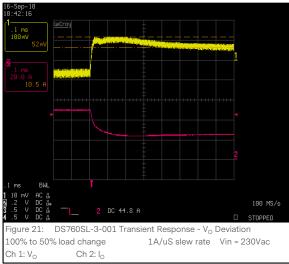
DS760SL-3-001 Performance Curves













Protection Function Specifications

Input Fuse

DS760SL series are equipped with an internal non user serviceable 10A High Rupturing Capacity (HRC) 250Vac fuse to IEC 127 for fault protection in both the L1 and L2 lines input.

Over Voltage / Under Voltage Protection (OVP / UVP)

The PSU overvoltage protection shall be locally sensed. The PSU shall shutdown in latched mode after an over voltage condition. This latch can be cleared by an AC power interruption.

OVP

Power supply latches off during output overvoltage, and restart by cycling the input or PSON/L, ON after a minimum OFF time of 1 second.

Note if the standby output (V_{SB}) was detected to be over-voltage and shutdown then the asserting edge of the PSON/L signal will re-enable the standby rail.

Parameter	Min	Nom	Max	Unit
V _O Output Overvoltage	13.3	/	14.5	V
5V _{SB} Output Overvoltage	5.75	/	6.40	V

UVP

If the Vo output is below the regulation band then the output Vo will be latched off and only restarted by cycling the input or remote enable, ON after a minimum OFF time of 1 second.

If V_{SB} falls below the regulation band the power supply will not latch this output off but Vo will be turned off until the V_{SB} is back within range.

Over Current Protection (OCP)

DS760SL series includes internal current limit circuitry to prevent damage in the event of over current or short circuit.

The Vo over-current protection is a latched off type. When the over load condition is removed, the power supply can be restart by cycling the AC line or PSON/L, ON after a minimum OFF time of 1 second to reset the latch..

The V_{SB} over-current protection is auto-recovery once the fault is removed.

Parameter	Min	Nom	Max	Unit
V _O Output Overcurrent	65.42	/	80.99	А
5V _{SB} Output Overvoltage	3.7	/	5.0	А



Short Circuit Protection (SCP)

If a short circuit condition occurs to main Vo output, the power supply main output Vo will shut down within 50ms in order to reduce the power that can be delivered into the short. The V_{SB} will remain ON.

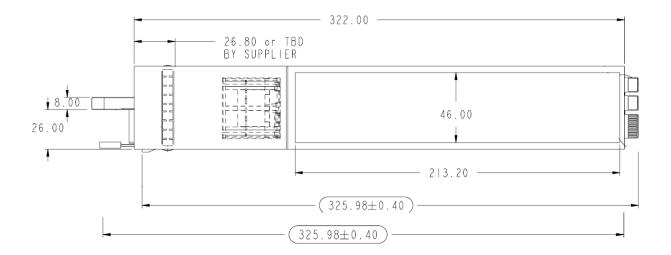
If a short circuit condition occurs to the V_{SB} output, the power supply will shut down with main output Vo turned off and the standby V_{SB} output will auto-recovery once the fault is removed.

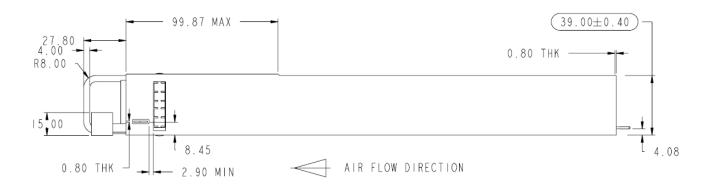
Over Temperature Protection (OTP)

The DS760SL series power supply incorporated thermal protection to prevent damage or degradation due to overheating. The power supply will turn off if there is an over temperature condition or if the output connector exceeds 100 degrees C. The output connector temp. sensor is located on the output connector PCB area. Once the temperature of the power supply or connector is reduced within the normal limit, the power supply will restart automatically.



Mechanical Outlines

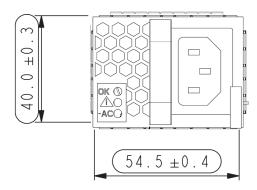


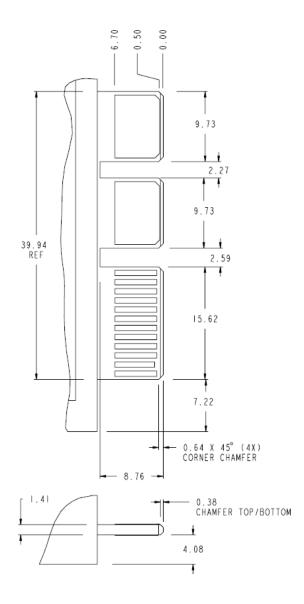






Mechanical Outlines







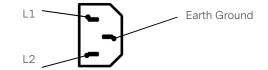
Connector Definitions

AC Input Connector

Pin 1 - L1

Pin 2 - L2

Pin 3 - Earth Ground



Output Connector - Power Blades

P1 - +12V P2 - +12V P3 - Ground P4 - Ground

Output Connector - Control Signals

S1 - +12V Sense S2 - +12V RTN Sense S3 - +12V Current Share S4 - SMB_ALERT/L

\$5 - \$DA \$6 - \$CL \$7 - P\$KILL \$8 - P\$ON/L \$9 - PW_OK \$10 - P\$_A1

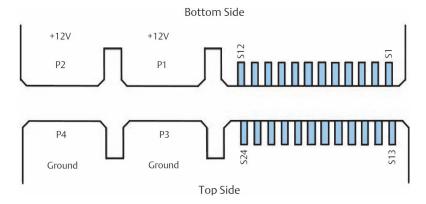
S11 - +5.0V_STBY (VSB) S12 - +5.0V_STBY (VSB)

S13 - Reserved S14 - PRESENT/L S15 - PS_A0 S16 - Reserved

S17 – Reserved for factory use

S18 - EEPROM_WP S19 - ACOK/H S20 - Not used S21 - Not used

S22 – Reserved for factory use
S23 – +5.0V_STBY (VSB)
S24 – +5.0V_STBY (VSB)



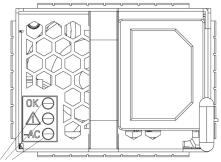


Power / Signal Mating Connectors and Pin Types

Table 5. Mating Connectors for DS760SL-3 Series					
Reference On Power Supply		Mating Connector or Equivalent			
AC Input Connector	IEC60320-C14	IEC60320-C13			
Output Connector	MOLEX P/N 45984005	MOLEX P/N 45984-4343			



LED Indicator Definitions



Three status LEDs located at the front panel of the power supply beside the AC inlet provide status signal indication.

LED	Function	Color
OK	DCOK	Green
	Fail	Yellow
~AC	ACOK	Green

Status LED

Summary of Status Signals, Registers and LED indicators

	Status	Signals	Status Register Shutdown register			LED status						
Conditions	ACOK /H	PWOK /H	PSON	PWOK	Fan Fail	AC- Loss	0- Temp	0- Current	Fail	AC	DC	Fail
Normal operation	1	1	1	1	0	0	0	0	0	On	On	Off
Vo 12V over current	1	0	1	0	0	0	0	1	1	On	Off	On
AC Input Fail	0	0	1	0	0	1	0	0	1	Off	Off	Off
Fan blocked or running under speed. O/P's ok	1	1	1	1	0	0	0	0	0	On	On	Off
UV on Vo 12V & PS has latched off	1	0	1	0	0	0	0	0	1	On	Off	On
UV on Vsb +5.0 and PS Has Turned O#	1	0	1	0	0	0	0	0	1	On	Off	On
OV on V1 12V or Vsb +5.0 & PS has latched O#	1	0	1	0	0	0	0	0	1	On	Off	On
Over Temp and PS has turned O#	1	0	1	0	0	0	1	0	1	On	Off	On
Fan below shutdown limit	1	0	1	0	1	0	0	0	1	On	Off	On
No problems but PS is in standby mode	1	0	0	0	0	0	0	0	0	On	Off	Off



Weight

The DS760SL series weight is 2.19 lbs maximum.



EMC Immunity

DS760SL-3 series power supply is designed to meet the following EMC immunity specifications.

Table 6. Environmental Specifications						
Document	Description					
EN61000-3-2: 1995	Electromagnetic compatibility (EMC) - Part 3: Limits Section 2: Limits for harmonic current emissions (equipment input current up to and including 16A Amendment A1:1998 per phase) Amendment A2: 1998 Amendment A14:2000					
EN61000-3-3: 1995	Electromagnetic compatibility (EMC) Part 3: Limits Section 3: Limitation of voltage fluctuations and flicker in low-voltage supply systems for equipment with rated current up to and including 16A.					
IEC1000-4 / 801	Industrial-Process Measurement and Control Equipment Immunity Requirements and Test Method.					
EN61000-4	Industrial-Process Measurement and Control Equipment Immunity Requirements and Test Method.					
EN61000-4-2: 1995	Electromagnetic compatibility (EMC) - Part 4: Testing and measurement techniques. Section 2: Electrostatic discharge immunity test. Basic EMC Publication.					
EN61000-4-3: 1995	Section 3: Radiated, radio frequency, electromagnetic field immunity test					
EN61000-4-4: 1995	Section 4: Electrical fast transient / Burst immunity test. Basic EMC Publication.					
EN61000-4-5: 1995	Section 5: Surge immunity test					
EN61000-4-6: 1995	Section 6: Immunity to conducted disturbances induced by radio frequency fields					
EN61000-4-8: 1995	Section 8: Power frequency magnetic field immunity test					
EN61000-4-11: 1995	Section 11: Voltage dips, short interruptions and voltage variations immunity tests					
CSA C108.8-M1983	Canadian Department of Communications Radio Interface Regulations					
VCCI	Voluntary Control Council for Interference, Japanese EMI Regulations					



Safety Certifications

The DS760SL power supply is intended for inclusion in other equipment and the installer must ensure that it is in compliance with all the requirements of the end application. This product is only for inclusion by professional installers within other equipment and must not be operated as a stand alone product.

Table 7. Safety Certifications f	Table 7. Safety Certifications for DS760SL Series Power Supply						
Document	File #	Description					
UL 60950-1 CSA-C22.2 No. 60950-1-03	E132002	United States and Canada Standard, Safety for information technology equipment.					
EN60950-1:A11/2004	B090313890540	Harmonized European Standard, Safety for information technology equipment.					
IEC60950-1		International Standard, Safety for Information Technology Equipment. (ITE)					
CB Certificate and Report	SG-OF-02936	(All CENELEC Countries)					
CHINA CCC Approval	2008010907283624	China Requirements					
BSMI	C1337061600869	Taiwan bureau of standards, metrology and inspection.					
GOST	8637846	Mandatory certification mark for all electrical products to be shipped into Russia					
IRAM	211-238023-300	Electrical & electronic equipment that meet Argentina's requirements					
KCC	AIL-7001497-J000(A)	Korea mandatory certification mark for all electrical products					
TUV	B091113890647	German Safety of Equipment Act.					
		The PSU will have Protective Earth and reinforced/double insulation between input and output. Work with TN supply systems.					



EMI Emissions

The DS760SL-3 series has been designed to comply with the Class A limits of EMI requirements.

Conducted Emissions (CISPR22, EN55032)

The DS760SL-3 series power supplies comply with the Class A limits for conducted emissions with a margin of 3dB or greater as calculated according to the statistical methods described in EN55032.

Radiated Emissions (CISPR22, EN55022)

The DS760SL-3 series power supplies comply with the Class A limits for radiated emissions with a margin of 3dB or greater.

AC Harmonic Current Emissions (IEC 61000-3-2)

The DS760SL-3 series power supplies meet the AC Harmonic Current Emission Class A limits as adjusted for input voltage.



Operating Temperature

The DS760SL-3 series power supplies will start and operate within stated specifications at the below ambient temperature and altitude conditions:

0 to 40°C from 0 to 1800 meters altitude without derating in any output

0 to 38°C from 1800 to 3000 meters altitude without derating in any output

0 to 60°C from 0 to 1800 meters altitude with $\rm V_{\rm O}$ derated to 40A and Vsb to 2.4A

0 to 40°C from 0 to 4000 meters altitude with $\rm V_{\rm O}$ derated to 45A and Vsb to 2.4A



Storage and Shipping Temperature / Humidity

The DS760SL-3 series power supplies can be stored or shipped at temperatures between -40°C to +85°C and relative humidity from 5% to 95% non-condensing.

Altitude

The DS760SL-3 series power supplies will operate within specifications at altitudes up to 4,000 meters with the output derating defined in operating temperature section.

The power supply can be stored at altitudes of up to 13,000 meters above sea level.

Humidity

The DS760SL-3 series power supplies will operate within specifications when subjected to a relative humidity from 7% to 93% non condensing.

The DS760SL-3 series power supplies can be stored in a relative humidity from 5% to 95% non-condensing.

Vibration

The DS760SL-3 series power supplies will pass the following vibration specifications:

Non-operational - 5G sine sweep from 5Hz to 500Hz, dwelling at resonant frequencies for 1 hour each.

Acoustic Noise Emissions

When operated with specified cooling under any steady-state or repetitive dynamic load within the range specified in this document the power supply will meet the requirements below:

Model	Acoustic Requirements
DS760SL-3	The measured A-weighted sound power level (LwA) will not exceed 69dBA at an ambient/inlet air temperature of $23\pm2^{\circ}$ C per ISO7779 and ISO9295. No prominent discrete tones will be emitted per ISO7779 Annex D, using a criterion of (Lt - Ln)³ 3dB. The frequency of repetition is defined as 10 < fREP < 1/(2 * tRESPONSE) Hz
DS760SL-3-001	N/A



POWER AND CONTROL SIGNAL DESCRIPTIONS

AC Input Connector

This connector supplies the AC Mains to the DS760SL power supply.

Pin1 - L1 Pin2 - L2 Pin3 - Earth Ground

Output Connector – Power Blades

These pins provide the main output for the DS760SL.

P1 - +12V P2 - +12V P3 - Ground P4 - Ground

Output Connector - Control Signals

The DS760SL series contains control signal header providing analogy control interface, standby power and I²C interface. These are control signals which are directly connected from the system to the power supply.

+12V Sense, +12V RTN Sense - (Pins S1, S2)

The main output of the DS760SL-3 is equipped with a remote sensing capability that will compensate for a power path drop around the entire loop of 100mV. This feature is implemented by connecting the +12V Sense (pin S1) and the +12V RTN Sense (pin S2) to the positive and negative rails of the main output, respectively, at a location that is near to the load. Care should be taken in the routing of the sense lines as any noise sources or additional filtering components introduced into the voltage rail may affect the stability of the power supply. The DS760SL-3 will operate appropriately without the sense lines connected, however it is recommended that the sense lines be connected directly to the main output terminals if remote sensing is not required. This remote sense circuit will not raise the power supply's output voltage to the OVP trip level. Main output remote sense has no effect on the standby output (V_{SB}).

+12V Current Share - (Pin S3)

Single wire parallel signal used for +12V output current sharing among the power supplies.

SMB_ALERT/L, SDA and SCL - (Pins S4, S5, S6)

Please refer to "Communication Bus Descriptions" section.

PSKILL - (Pin S7)

This signal pin should be grounded in the system. If left open, power supply operation will be inhibited (Standby V_{SB} output will remain on).

PSON/L - (Pin S8)

This signal input pin controls the normal turning ON and Off of the +12V of the DS760SL-3 power supply. The power supply main output (V_O) will be enabled when this signal is pulled low, below 0.8V. The Power supply output (except V_{SB} output) will be disabled when this input is driven higher than 2.0V, or left open circuited.



POWER AND CONTROL SIGNAL DESCRIPTIONS

PW_OK - (Pin S9)

The PW_OK is an output signal driven high, by the power supply to indicate that all outputs are valid. If any of the power supply outputs fails below its regulation limits, this output will be driven low. The output signal is an open drain output internally pulled up in the power supply to internal standby supply 5.0V via a 1K ohm resistor. It is capable of driving the output below 0.4V with a load of 4mA.

PS_A1, PS_A0 - (Pins S10, S15)

Please refer to "Communication Bus Descriptions" section.

+5.0V_STBY - (Pins S11, S12, S23, S24)

The DS760SL-3 provides a regulated 5.0 volt 2.4 amp auxiliary output voltage to power critical circuitry that remain active regardless of the on/off status of the power supply's main output. The standby output (V_{SB}) voltage is available whenever a valid AC input voltage is applied to the unit. The standby output is independently short circuit protected and is referenced to the main +12V output ground (P3, P4).

Reserved, Not Used - (Pins S13, S16, S17, S20, S21, S22)

These pins are reserved and might be connected internally in the power supply. No externally connection should be make to these pins.

PRESENT/L - (Pins S14)

This signal pin is connected to +12V output ground inside the power supply. This pin is to be pull high on the system side by a resistor of 4.7K or higher. A TTL logic LOW indicates the power supply is inserted and seated into the system power supply connector. A logic HIGH indicated the removal of the power supply.

EEPROM_WP - (Pin S18)

This signal is pulled up to internal standby 5.0V by a 3.74k resistor in the power supply to prevent data in the EEPROM from being over-written. If this signal is pulled down by the system, write cycles to the EEPROM are permitted.

ACOK/H - (Pin S19)

The ACOK signal is a normally HIGH level TTL logic signal when the AC input voltage is within the allowable limits. A TTL logic LOW level, with a 7mS early warning will be sent before the main output loses regulation. This signal is an open drain output internally pulled up in the power supply 5.0V via a 1K ohm resistor. It is capable of driving the output below 0.4V with a load of 4mA.



I²C Bus Signals

The DS760SL-3 power supply contains enhanced monitoring and control functions implemented via the I²C bus. The DS760SL-3 I²C functionality (PSMI and FRU data) can be accessed via the output connector control signals. The communication bus is powered either by the internal standby supply or from an external power source connected to the 5.0V STBY (ie: accessing an unpowered power supply as long as the standby output of another power supply connected in parallel is on).

If units are connected in parallel or in redundant mode, the 5.0V STBY (VSB) must be connected together in the system. Otherwise, the I²C bus will not work properly when a unit is inserted into the system without the AC source connected.

SMB_ALERT/L - (Pin S4)

Interrupt signal indicating system should check the power supply status and warnings. This signal is an open drain output from the power supply. A pull up resistor should be located on the system side to standby V_{SR} Output.

SDA and SCL - (Pins S5, S6)

I²C serial data and clock bus - these pins are internally pulled up to 3.3V with a 100K resistor.

PS_A0, PS_A1 (I²C Address BIT 0, BIT1 Signals) - (Pins S15, S10)

These two input pins are the address lines A0 and A1 to indicate the slot position the power supply occupies in the power bay and define the power supply addresses for FRU data and PSMI data communication. This allows the system to assign different addresses for each power supply. During I²C communication between system and power supplies, the system will be the master and power supplies will be slave.

They are internally pulled up to internal standby supply with a 10K resistor.

I²C Bus Communication Interval

The interval between two consecutive I^2C communications to the power supply should be at least 200us to ensure proper monitoring functionality.

I²C Bus Signal Integrity

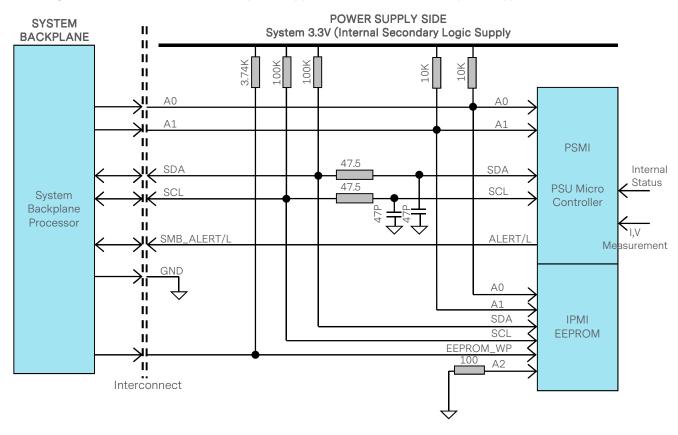
The noise on the I²C bus (SDA, SCL lines) due to the power supply will be less than 500mV peak to peak. This noise measurement should be made with an oscilloscope bandwidth limited to 100MHz. Measurements should be make at the power supply output connector with 3.2K ohm resistors pulled up to standby output and 20pf ceramic capacitors to standby output return.

The noise on the address lines A0 and A1 will be less than 100mV peak-to-peak. This noise measurement should be made at the power supply output connector.



I²C Bus Internal Implementation, Pull-ups and Bus Capacitances

These signals are directly connected from the power supply(s) to system or each of the power supplies within system.



I²C Bus - Recommended external pull-ups

Electrical and interface specifications of I²C signals (referenced to standby output return pin, unless otherwise indicated):

Parameter	Condition	Symbol	Min	Туре	Max	Unit
SDA, SCL Internal Pull-up Resistor		R _{int}	-	100	-	Kohm
SDA, SCL Internal Bus Capacitance		C _{int}	-	47	-	pF
Recommended External Pull-up Resistor	1 PSU	R _{ext}	-	1.0	-	Kohm
Recommended External Pull-up Resistor	2 PSU	R _{ext}	-	0.5	-	Kohm

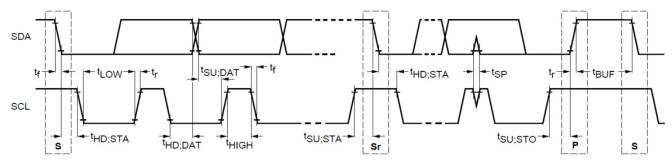


Logic Levels

DS760SL-3 series power supply I²C communication bus will respond to logic levels as per below:

Logic High: 5.0V nominal (Spec is 2.1V to 5.5V)** Logic Low: 500mV nominal (Spec is 800mV max)**

Timings



Danamatan	Complete	Standard-Mode Specs		A street Management		Unit	
Parameter	Symbol	Min	Max	Actual N	Actual Measured		
SCL clock frequency	f _{SCL}	0	100	96	96.8		
Hold time (repeated) START condition	t _{HD;STA}	4.0	-	4	.3	uS	
LOW period of SCL clock	t _{LOW}	4.7	-	13	3.5	uS	
HIGH period of SCL clock	t _{HIGH}	4.0	50	4.4		uS	
Setup time for repeated START condition	t _{su;sta}	4.7	-	5.83		uS	
Data hold time	t _{HD;DAT}	0	3.45	1.87		uS	
Data setup time	t _{su;dat}	250	-	5765		nS	
Rise time	t _r	-	1000	SCL = 972 SDA = 98		nS	
Fall time	t _f	-	300	SCL = 148.5	SDA = 148	nS	
Setup time for STOP condition	t _{su;sto}	4.0	-	6.36		uS	
Bus free time between a STOP and START condition	t _{BUF}	4.7	-	10	00	uS	

^{***}Note - Artesyn 73-769-001 $\mbox{\sc l}^2\mbox{\sc C}$ adapter (USB-to- $\mbox{\sc l}^2\mbox{\sc C}$) and Universal PMBus GUI software was used.



^{**} Note - Artesyn 73-769-001 I²C adapter was used.

Device Addressing

The DS760SL series will respond to supported commands on the I²CTM bus that are addressed according to pins A1 and A0 pins of output connector.

Address pins are held HIGH by default via pulled up to internal standby supply with a 10K resistor. To set the address as "0", the corresponding address line should be pulled down to logic ground level. Below table show the address of the power supply with A0 and A1 pins set to either "0" or "1":

DOLL CLAA	Slot II	Slot ID Bits		IPMI EEPROM	
PSU Slot	A1	A0	PMBus™ Address	(FRU) Read Address	
1	0	0	0xB0	0xA0	
2	0	1	0xB2	0xA2	
3	1	0	0xB4	0xA4	
4	1	1	0xB6*	0xA6*	

Note: Default I²C address when A0 and A1 are left open.



System Management bus

Power Supply System Management Bus will be accessible within the following delays from events visible to the system.

Any EEPROM devices, measurement ports or other features will be accessible and valid with the same timing as for the status port.

Signal timing - status signals and ports

Event	Time	Max	Notes
AC applied to this PS, no	AC Input to status valid.	1.0s	AC input to status signals valid.
other shared power sources	AC Input to ports valid.	1.0s	AC input to status, control and measurement ports accessible and valid.
External shared power	Shared Power to Status valid.	1.0s	Shared power to status signals valid.
source provided	Shared Power to ports valid.	1.0s	Shared power to status, control and measurement ports accessible and valid.
PS inserted into active	PRESENT to ON status valid.	1.0s	Hot plug to status signals valid.
system	PRESENT to ON ports valid.	1.0s	Hot plug to status, control and measurement ports accessible and valid
PS turned on	STANDBY to ON status valid.	1.0s	PSON/L to status signals valid for ON condition.
To turned on	STANDBY to ON ports valid.	1.0s	PSON/L to status and measurement ports valid for ON condition.



FRU (EEPROM) Data

The FRU (Field Replaceable Unit) data format is compliant with the Intel IPMI v1.0 specification. The DS760SL-3 uses 1 page of EEPROM for FRU purpose. The one page of EEPROM contains up to 256 byte-sized data locations.

Where: OFFSET denotes the address in decimal format of a particular data byte within

DS760SL-3 EEPROM.

VALUE -The VALUE details data written to a particular memory location of the EEPROM.

DEFINITION -The contents DEFINITION refers to the definition of a particular data byte.

OF	FSET	DEFINITION	SPEC	VALUE
(DEC)	(HEX)	(REMARKS)	(DEC)	(HEX)
		COMMON HEADER, 8 BYTES		
0	00	FORMAT VERSION NUMBER (Common Header)	1	01
1	01	INTERNAL USE AREA OFFSET (In multiples of 8 Bytes)	24	18
2	02	CHASSIS INFO AREA OFFSET (In multiples of 8 Bytes)	1	01
3	03	BOARD INFO AREA OFFSET (Not used)	0	00
4	04	PRODUCT INFO AREA OFFSET (In multiples of 8 Bytes)	5	05
5	05	MULTI RECORD AREA OFFSET (In multiples of 8 Bytes)	15	0F
6	06	PAD (Reserved - always 00H)	0	00
7	07	ZERO CHECK SUM (256 - (Sum of bytes 000d to 006d))	210	D2
		CHASSIS INFO AREA (32 BYTES)		
8	08	FORMAT VERSION NUMBER (Default value is 1.)	1	01
9	09	CHASSIS INFO AREA LENGTH (Default value is 0.)	0	00
10	0A	CHASSIS TYPE (Default value is 0.)	0	00
11	0B	CHASSIS PART NUMBER Type/Length 10 byte allocation OCAH (if used) (Default value is 0.)	0	00
12	OC OC	CHASSIS PART NUMBER BYTES (Default value is 0.)	0	00
13	0D	CHASSIS FART NOMBER BTTES (Delault value is 0.)	0	00
14	0E		0	00
15	0F		0	00
16	10		0	00
17	11		0	00
18 19	12 13		0	00
20	14		0	00
21	15		0	00
22	16	CHASSIS SERIAL NUMBER Type/Length 15 bytes allocation 0CFH (if used) (Default value is 0.)	207	CF
23	17	CHASSIS SERIAL NUMBER BYTES (Default value is 0.)	0	00
24	18		0	00
25	19		0	00
26	1A		0	00
27	1B		0	00
28	1C		0	00
29 30	1D 1E		0	00 00
31	1F		0	00
32	20		0	00
33	21		0	00
34	22		0	00
35	23		0	00
36	24		0	00
37	25		0	00



OFF	OFFSET DEFINITION		SPEC VALUE	
(DEC)	(HEX)	(REMARKS)	(DEC)	(HEX)
38	26	End Tag (0C1h if used)	0	00
39	27	CHKSUM (From 08d to 38d if used)	255	FF
		PRODUCT INFORMATION AREA, 80 BYTES		
40	28	FORMAT VERSION NUMBER	1	01
41	29	PRODUCT INFO AREA LENGTH (In multiples of 8 bytes) 80 bytes are allocated. 80-Byte / 8 = 0AH.	10	0A
42	2A	Language (English = 19H)	25	19
43	2B	MANUFACTURER NAME TYPE / LENGTH (0C7H) 7:6 - (11)b, 8-Bit ASCII+Latin 1, 5:0 - (000111)b, 7-Byte Allocation	199	C7
44 45 46 47 48 49	2C 2D 2E 2F 30 31	MANUFACTURER NAME "E" = 45H "M" = 4DH "E" = 45H "R" = 52H "S" = 53H "O" = 4FH "N" = 4EH	69 77 69 82 83 79 78	45 4D 45 52 53 4F 4E
51	33	PRODUCT NAME Type/Length (0CEH) 7-6: (11)b, 8-Bit ASCII+LATIN1, 5-0: (000110)b, 14-Byte Allocation	206	CE
52 53 54 55 56 57 58 59 60 61 62 63 64 65	34 35 36 37 38 39 3A 3B 3C 3D 3E 3F 40 41	Product Name "D" = 44H "S" = 53H "7" = 37H "6" = 36H "0" = 30H "S" = 53H "L" = 4CH " -" = 2DH "3" = 33H	68 83 55 54 48 83 76 45 51 00 00 00	44 53 37 36 30 53 4C 2D 33 00 00 00
66	42	PRODUCT PART/MODEL NUMBER Type/Length (0CAH) 7-6: (11)b, 8-Bit ASCII+LATIN1, 5-0: (000110)b, 6-Byte Allocation	PER	UNIT
67 68 69 70 71 72	43 44 45 46 47 48	POWER SUPPLY SPARE KIT NUMBER NOT APPLICABLE	00 00 00 00 00 00	00 00 00 00 00 00
73	49	PRODUCT VERSION NUMBER Type/Length (0C2H) 7-6: (11)b, 8-Bit ASCII+LATIN1, 5-0: (000010)b, 2-Byte Allocation	194	C2
74 75	4A 4B	*SHOULD TRACK MODEL REVISION indicated on BOM		UNIT UNIT
76	4C	PRODUCT SERIAL NUMBER Type/Length (OCDH) *PRODUCT SERIAL NUMBER IS BASED ON ASTEC SERIAL NUMBER FORMAT P/N: 41700201000 7-6: (11)b, 8-Bit ASCII+LATIN1, 5-0: (001101)b, 13-Byte Allocation	205	CD



OFFSET DEF		DEFINITION	SPEC '	VALUE
(DEC)	(HEX)	(REMARKS)	(DEC)	(HEX)
		PRODUCT SERIAL NUMBER: Model ID		
77	4D	"1" = 49H	73	49
78	4E	"0" = 49H	48	30
79 80	4F 50	"8" = 49H "0" = 49H	56 48	38 30
81	51	PRODUCT SERIAL NUMBER: MANUFACTURING YEAR AND WEEK		UNIT
82	52	CODE		UNIT
		*REFER TO 4170020100 FOR DETAILS		
83	53	PRODUCT SERIAL NUMBER: UNIQUE SERIAL NUMBER	PFR	UNIT
84	54	*REFER TO EN2274B FOR DETAILS		UNIT
85	55	NEI ER TO ENZZITADI OR DETINIES		UNIT
86	56		PER	UNIT
87	57	PRODUCT SERIAL NUMBER: MODEL REVISION	PER	UNIT
88	58	*SHOULD TRACK MODEL REVISION indicated on BOM	PER	UNIT
		PRODUCT SERIAL NUMBER MANUFACTURING LOCATION * REFER TO EN2274B FOR DETAILS		
89	59	"Z" = 5AH (Z for ZhongShan China)	90	5A
90	5A	ASSET TAG	200	C8
		7-6: (11)b, 8-Bit ASCII+LATIN1,		
		5-0: (001000)b, 8-Byte Allocation		
91	5B	NO ASSET TAG	00	00
92	5C		00	00
93	5D		00	00
94 95	5E 5F		00 00	00 00
96	60		00	00
97	61		00	00
98	62		00	00
99	63	FRU FILE ID	209	D1
		7-6: (11)b, 8-Bit ASCII+LATIN1,		
		5-0: (010001)b, 17-Byte Allocation REFER TO IPS FOR LATEST FRU FILE NAME		
100	0.4	"D"= 44H	60	4.4
100 101	64 65	"S"= 53H	68 83	44 53
102	66	"7"= 37H	55	37
103	67	"6"= 36H	54	36
104	68	"0"= 30H	48	30
105	69	"S" = 53H	83	53
106	6A 6B	"L"= 4CH " -"= 2DH	76	4C 2D
107 108	9C	"3"= 33H	45 51	33
109	6D	"R"= 52H "Should track latest FRU File ID on Spec. 1.1"	82	52
110	6E	"E"= 45H	69	45
111	6F	"V"= 56H	86	56
112	70	"1 "= 31H	PER	UNIT
113	71 72	"C"= 43H	PER	UNIT
114 115	72		00 00	00 00
116	74		00	00
117	75	END OF FIELD MARKER	193	C1
118	76	RESERVED	00	00
119	77	ZERO CHECK SUM (256-(Sum of bytes 40d to 118d))	PER	
110	1 1		1 111	0.111



OFF	SET	DEFINITION	SPEC '	VALUE
(DEC)	(HEX)	(REMARKS)	(DEC)	(HEX)
		MULTI RECORD AREA: Power Supply Information 72 Bytes		
		POWER SUPPLY RECORD HEARDER		
120	78	RECORD TYPE ID (0X00 = Power Supply Information)	00	00
121	79	7: (0)b, End of List 6-4: (000)b, Reserved 3-0: (0010)b, Record Format Version	02	02
122	7A	RECORD LENGTH: 24 Bytes	24	18
123	7B	RECORD CHECKSUM (Zero Checksum From 125d to 148d)	69	45
124	7C	HEADER CHECKSUM (Zero Checksum From 120d to 123d)	161	A1
		POWER SUPPLY RECORD		
125 126	7D 7E	Overall Capacity (Watts) 15-12: (0000)b, reserved 11-0: (1011111000)b, 760W = 02F8H Stored with LSB first then MSB	248 002	F8 02
127 128	7F 80	Peak VA (Watts) 15-12: (0000)b, reserved 11-0: (1101110000)b, 880W =0370H Stored with LSB first then MSB	112 003	70 03
129	81	INRUSH CURRENT (Amps) 25Amps = 19H	25	19
130	82	INRUSH INTERVAL (ms) 200ms = C8H	200	C8
131 132	83 84	LOW END INPUT VOLTAGE RANGE 1 90V = 9000(×10mV) = 2328H STORED WITH LSB FIRST THEN MSB	40 35	28 23
133 134	85 86	HIGH END INPUT VOLTAGE RANGE 1 264V = 26400(×10mV) = 6720H STORED WITH LSB FIRST THEN MSB	32 103	20 67
135 136	87 88	LOW END INPUT VOLTAGE RANGE 2 0V = 0(×10mV) = 0H, no voltage range 2 STORED WITH LSB FIRST THEN MSB	00 00	00 00
137 138	89 8A	HIGH END INPUT VOLTAGE RANGE 2 0V = 0(×10mV) = 0H, no voltage range 2 STORED WITH LSB FIRST THEN MSB	00 00	00 00
139	8B	LOW END INPUT FREQUENCY RANGE, 47Hz = 2FH	47	2F
140	8C	HIGH END INPUT FREQUENCY RANGE, 63Hz = 3FH	63	3F
141	8D	A/C DROPOUT TOLERANCE IN ms, 12ms = 0CH	12	0C
142	8E	BINARY FLAGS 7-5: (000)b, reserved 4: (1)b, Tachometer Pulses per Rotation / Predictive Fail Polarity (2 Pulses Per Rotation = 1; 1 Pulse Per Rotation = 0) OR (Signal Asserted (1) Indicates Failure = 0, Signal De-asserted (0) Indicates Failure = 1) 3: (1)b, Hot Swap / Redundancy Support 2: (0)b, Auto Switch Support 1: (1)b, Power Factor Correction Support 0: (0)b, Predictive Fail Support	27	1B
143 144 145	8F 90 91	Peak Wattage Capacity and Holdup Time 15-12: (0000)b, 12 mSeconds = 0CH 11-0: (1001011000)b, 760Watts = 02F8H Stored with LSB first then MSB.	12 248 002	0C F8 02
146	92	Combined Wattage	00	00



OFF	SET	DEFINITION	SPEC '	VALUE
(DEC)	(HEX)	(REMARKS)	(DEC)	(HEX)
148	94	PREDICTIVE FAIL TACHOMETER LOWER THRESHOLD Not applicable	00	00
		12V DC OUTPUT RECORD HEADER		
149	95	RECORD TYPE ID (0X01 = DC OUPUT)	001	01
150	96	End of List/Record Format Version Number 7: (0)b, End of List 6-4: (000)b, reserved 3-0: (0010)b, record format version	002	02
151	97	Record Length: 13 Bytes	13	0D
152	98	Record Checksum (Zero Checksum From 154d to 166d)	28	1C
153	99	Header Checksum (Zero Checksum From 149d to 152d)	212	D4
		+12V DC OUTPUT RECORD		
164	9A	+12V Output Information 7: (0)b, standby 6-4: (000)b, reserved 3-0: (0001)b, output number 1 = 001b	001	01
		NOMINAL VOLTAGE		
155 156	9B 9C	12.00V = 1200 (x10mV) = 04B0H Stored with LSB first then MSB.	176 004	B0 04
157 158	9D 9E	Maximum Negative Voltage Deviation 11.88V = 1188 (x10mV) = 04A4H. Stored with LSB first then MSB.	164 004	A4 04
159 160	9F A0	Maximum Positive Voltage Deviation 12.12V = 1212 (x10mV) = 04BCH Stored with LSB first then MSB.	188 004	BC 04
161 162	A1 A2	Ripple And Noise pk-pk 10Hz to 30MHz (mV) 100mV = 0064H Stored with LSB first then MSB.	100 000	64 00
163 164	A3 A4	Minimum Current Draw (10mA) 5.0A = 500 (x10mA) = 01F4H Stored with LSB first then MSB.	244 001	F4 01
165 166	A5 A6	Maximum Current Draw (10mA) 62.3A = 6230 (x10mA) = 1856H Stored with LSB first then MSB.	086 024	56 18
		5V0SB DC OUTPUT RECORD HEADER		
167	A7	Record Type ID (0x01 = DC Output)	001	01
168	A8	End of List/Record Format Version Number 7: (1)b, End of List 6-4: (000)b, reserved 3-0: (0010)b, record format version	130	82
169	A9	Record Length: 20 Bytes	001	01
170	AA	Record Checksum (Zero Checksum From 172d to 191d)	074	4A
171	AB	Header Checksum (Zero Checksum From 167d to 170d)	031	1F
		5V0SB DC OUTPUT RECORD		
172	AC	5V0SB Output Information 7: (1)b, Standby (Bit = 1 to indicate standby output) 6-4: (000)b, reserved 3-0: (0010)b, output number 2 = 010b	130	82
173 174	AD AE	Nominal Voltage 5.00V = 500 (x10mV) = 01F4H Stored with LSB first then MSB.	244 001	F4 01



DS760SL-3 series FRU (EEPROM) Data:

OFFSET		DEFINITION	SPEC	SPEC VALUE			
(DEC)	(HEX)	(REMARKS)	(DEC)	(HEX)			
		Maximum Negative Voltage Deviation					
175	AF	5.25V = 525 (x10mV) = 020DH	013	0D			
176	В0	Stored with LSB first then MSB.	002	02			
		Maximum Positive Voltage Deviation					
177	B1	4.75V = 475 (x10mV) = 01DBH	219	DB			
178	B2	Stored with LSB first then MSB.	001	01			
		Ripple And Noise pk-pk 10Hz to 30MHz (mV)					
179	B3	100mV = 0064H	100	64			
180	B4	Stored with LSB first then MSB.	000	00			
		Minimum Current Draw (10mA)					
181	B5	000 = 0000H	000	00			
182	В6	Stored with LSB first then MSB.	000	00			
		Maximum Current Draw (10mA)					
183	B7	2.40A = 240(x 10mA) = 00F0H	240	F0			
184	B8	Stored with LSB first then MSB.	000	00			
185	B9	Reserved	00	00			
186	ВА	Reserved	00	00			
187	BB	Reserved	00	00			
188	ВС	Reserved	00	00			
189	BD	Reserved	00	00			
190	BE	Reserved	00	00			
	BF						
191	BF	Reserved	00	00			
	1	INTERNAL USE AREA, 64 bytes		1			
100	00	Format Version Number	001	01			
192	C0	7:4 -reserved, write as 0000b 3:0 -format version number = 1h for this specification.	001	01			
193	01	3.0 -ioimat version number - in ioi tilis specification.	0	00			
193	C1 C2		0	00			
195	C3		0	00			
196	C4		0	00			
197	C5		0	00			
198	C6		0	00			
199	C7		0	00			
200	C8		0	00			
201	C9		0	00			
202	CA		0	00			
203	СВ		0	00			
204	CC		0	00			
205	CD		0	00			
206	CE		0	00			
207	CF		0	00			
208	D0		0	00			
209	D1		0	00			
210	D2		0	00			
211	D3		0	00			
212	D4		0	00			
213	D5		0	00			
214	D6		0	00			
215	D7		0	00			
216	D8		0	00			
217	D9		0	00			
218	DA		0	00			
219	DB		0	00			
220	DC		0	00			



DS760SL-3 series FRU (EEPROM) Data:

OFFSET		DEFINITION	SPEC	VALUE
(DEC)	(HEX)	(REMARKS)	(DEC)	(HEX)
221	DD		0	00
222	DE		0	00
223	DF		0	00
224	E0		0	00
225	E1		0	00
226	E2		0	00
227	E3		0	00
228	E4		0	00
229	E5		0	00
230	E6		0	00
231	E7		0	00
232	E8		0	00
233	E9		0	00
234	EA		0	00
235	EB		0	00
236	EC		0	00
237	ED		0	00
238	EE		0	00
239	EF		0	00
240	F0		0	00
241	F1		0	00
242	F2		0	00
243	F3		0	00
244	F4		0	00
245	F5		0	00
246	F6		0	00
247	F7		0	00
248	F8		0	00
249	F9		0	00
250	FA		0	00
251	FB		0	00
252	FC		0	00
253	FD		0	00
254	FE		0	00
255	FF	CHECKSUM: (From 192 to 254 if used)	PER	UNIT



FRU (EEPROM) Data

The FRU (Field Replaceable Unit) data format is compliant with the Intel IPMI v1.0 specification. The DS760SL-3-001 uses 1 page of EEPROM for FRU purpose. The one page of EEPROM contains up to 256 byte-sized data locations.

Where: OFFSET denotes the address in decimal format of a particular data byte within

DS760SL-3-001 EEPROM.

VALUE -The VALUE details data written to a particular memory location of the EEPROM.

DEFINITION -The contents DEFINITION refers to the definition of a particular data byte.

OF	FSET	DEFINITION	SPEC	VALUE
(DEC)	(HEX)	(REMARKS)	(DEC)	(HEX)
		COMMON HEADER, 8 BYTES		
0	00	FORMAT VERSION NUMBER (Common Header)	1	01
1	01	INTERNAL USE AREA OFFSET (In multiples of 8 Bytes)	24	18
2	02	CHASSIS INFO AREA OFFSET (In multiples of 8 Bytes)	1	01
3	03	BOARD INFO AREA OFFSET (Not used)	0	00
4	04	PRODUCT INFO AREA OFFSET (In multiples of 8 Bytes)	5	05
5	05	MULTI RECORD AREA OFFSET (In multiples of 8 Bytes)	15	0F
6	06	PAD (Reserved - always 00H)	0	00
7	07	ZERO CHECK SUM (256 - (Sum of bytes 000d to 006d))	210	D2
		CHASSIS INFO AREA (32 BYTES)		
8	08	FORMAT VERSION NUMBER (Default value is 1.)	1	01
9	09	CHASSIS INFO AREA LENGTH (Default value is 0.)	0	00
10	0A	CHASSIS TYPE (Default value is 0.)	0	00
11	0B	CHASSIS PART NUMBER Type/Length 10 byte allocation 0CAH (if used) (Default value is 0.)	0	00
12	0C	CHASSIS PART NUMBER BYTES (Default value is 0.)	0	00
13	0D		0	00
14 15	0E 0F		0	00 00
16	10		0	00
17	11		0	00
18	12		0	00
19	13		0	00
20	14		0	00
21	15		0	00
22	16	CHASSIS SERIAL NUMBER Type/Length 15 bytes allocation 0CFH (if used) (Default value is 0.)	0	00
23	17	CHASSIS SERIAL NUMBER BYTES (Default value is 0.)	0	00
24	18		0	00
25	19		0	00
26	1A		0	00
27 28	1B 1C		0	00 00
29	1D		0	00
30	1E		0	00
31	1F		0	00
32	20		0	00
33	21		0	00
34	22		0	00
35	23		0	00
36	24		0	00
37	25		0	00



DS760SL-3-001 FRU (EEPROM) Data:

OFF	SET	DEFINITION	SPEC '	VALUE
(DEC)	(HEX)	(REMARKS)	(DEC)	(HEX)
38	26	End Tag (0C1h if used)	0	00
39	27	CHKSUM (From 08d to 38d if used)	255	FF
		PRODUCT INFORMATION AREA, 80 BYTES		
40	28	FORMAT VERSION NUMBER	1	01
41	29	PRODUCT INFO AREA LENGTH (In multiples of 8 bytes) 80 bytes are allocated. 80-Byte / 8 = 0AH.	10	0A
42	2A	Language (English = 19H)	25	19
43	2B	MANUFACTURER NAME TYPE / LENGTH (0C7H) 7:6 - (11)b, 8-Bit ASCII+Latin 1, 5:0 - (000111)b, 7-Byte Allocation	199	C7
44 45 46 47 48 49 50	2C 2D 2E 2F 30 31 32	MANUFACTURER NAME "E" = 45H "M" = 4DH "E" = 45H "R" = 52H "S" = 53H "O" = 4FH "N" = 4EH PRODUCT NAME Type/Length (0CEH)	69 77 69 82 83 79 78	45 4D 45 52 53 4F 4E
	00	7-6: (11)b, 8-Bit ASCII+LATIN1, 5-0: (000110)b, 14-Byte Allocation	200	OL.
52 53 54 55 56 57 58 59 60 61 62 63 64 65	34 35 36 37 38 39 3A 3B 3C 3D 3E 3F 40 41	Product Name "D"= 44H "S"= 53H "7"= 37H "6"= 36H "0"= 30H "S"= 53H "L"= 4CH "-"= 2DH "3"= 33H "-"= 2DH "0"= 30H "0"= 30H "1"= 31H PRODUCT PART/MODEL NUMBER Type/Length (0CAH) 7-6: (11)b, 8-Bit ASCII+LATIN1, 5-0: (000110)b, 6-Byte Allocation	68 83 55 54 48 83 76 45 51 45 48 48 49 00	44 53 37 36 30 53 4C 2D 33 2D 30 30 31 00
67 68 69 70 71 72	43 44 45 46 47 48	POWER SUPPLY SPARE KIT NUMBER NOT APPLICABLE	00 00 00 00 00 00	00 00 00 00 00 00
73	49	PRODUCT VERSION NUMBER Type/Length (0C2H) 7-6: (11)b, 8-Bit ASCII+LATIN1, 5-0: (000010)b, 2-Byte Allocation	194	C2
74 75	4A 4B	PRODUCT VERSION NUMBER / AUTO REV *SHOULD TRACK MODEL REVISION indicated on BOM	PER	UNIT UNIT
76	4C	PRODUCT SERIAL NUMBER Type/Length (0CDH) *PRODUCT SERIAL NUMBER IS BASED ON ASTEC SERIAL NUMBER FORMAT P/N: 41700201000 7-6: (11)b, 8-Bit ASCII+LATIN1, 5-0: (001101)b, 13-Byte Allocation	205	CD

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OF	FSET	DEFINITION	SPEC	VALUE
(DEC)	(HEX)	(REMARKS)	(DEC)	(HEX)
		PRODUCT SERIAL NUMBER: Model ID		
77	4D	"1" = 47H	73	49
78	4E	"1" = 31H	49	31
79	4F	"3" = 33H	51	33
80	50	"1" = 31H	49	31
81	51	PRODUCT SERIAL NUMBER: MANUFACTURING YEAR AND WEEK	PER	UNIT
82	52	CODE	PER	UNIT
		*REFER TO 4170020100 FOR DETAILS		
83	53	PRODUCT SERIAL NUMBER: UNIQUE SERIAL NUMBER	PER	UNIT
84	54	*REFER TO 4170020100 FOR DETAILS	PER	UNIT
85	55			UNIT
86	56		PER	UNIT
87	57	PRODUCT SERIAL NUMBER: MODEL REVISION	PER	UNIT
88	58	*SHOULD TRACK MODEL REVISION indicated on BOM	PER	UNIT
		PRODUCT SERIAL NUMBER MANUFACTURING LOCATION *REFER TO EN2274B FOR DETAILS		
89	59	"Z" = 5AH (Z for ZhongShan China)	90	5A
90	5A	ASSET TAG	200	C8
		7-6: (11)b, 8-Bit ASCII+LATIN1,		
		5-0: (001000)b, 8-Byte Allocation		
91	5B	NO ASSET TAG	00	00
92	5C		00	00
93	5D		00	00
94	5E		00	00
95	5F		00	00
96 97	60 61		00	00
98	62		00 00	00 00
99	63	FRU FILE ID	209	D1
99	03	7-6: (11)b, 8-Bit ASCII+LATIN1,	209	DI
		5-0: (010001)b, 17-Byte Allocation		
		REFER TO IPS FOR LATEST FRU FILE NAME		
100	64	"D"= 44H	68	44
101	65	"S"= 53H	83	53
102	66	"7"= 37H	55	37
103	67	"6"= 36H	54	36
104	68	"0"= 30H	48	30
105	69	"S"= 53H	83	53
106	6A	"L"= 4CH "-"= 2DH	76	4C
107	6B		45 51	2D
108 109	6C 6D	"3"= 33H "-"= 2DH	51 45	33 2D
110	6E	"0"= 30H	48	30
111	6F	"0"= 30H	48	30
112	70	"1"= 31H	49	31
113	71	"R"= 52H "Should track latest FRU File ID on Spec. 1.1"	82	52
114	72	"E"= 45H	69	45
115	73	"V"= 56H	86	56
116	74	"B"= 42H	PER	UNIT
117	75	END OF FIELD MARKER	193	C1
118	76	RESERVED	00	00
119	77	ZERO CHECK SUM (256-(Sum of bytes 40d to 118d))	PER	UNIT



OFF	SET	DEFINITION	SPEC \	/ALUE
(DEC)	(HEX)	(REMARKS)	(DEC)	(HEX)
		MULTI RECORD AREA: Power Supply Information 72 Bytes		
		POWER SUPPLY RECORD HEARDER		
120	78	RECORD TYPE ID (0X00 = Power Supply Information)	00	00
121	79	7: (0)b, End of List 6-4: (000)b, Reserved 3-0: (0010)b, Record Format Version	02	02
122	7A	RECORD LENGTH: 24 Bytes	24	18
123	7B	RECORD CHECKSUM (Zero Checksum From 125d to 148d)	63	3F
124	7C	HEADER CHECKSUM (Zero Checksum From 120d to 123d)	167	A7
		POWER SUPPLY RECORD		
125 126	7D 7E	Overall Capacity (Watts) 15-12: (0000)b, reserved 11-0: (1001011000)b, 600W =0258H Stored with LSB first then MSB	88 02	58 02
127 128	7F 80	Peak VA (Watts) 15-12: (0000)b, reserved 11-0: (1010110111)b, 695W =02B7H Stored with LSB first then MSB	183 002	B7 02
129	81	INRUSH CURRENT (Amps) 25Amps = 19H	25	19
130	82	INRUSH INTERVAL (ms) 200ms = C8H	200	C8
131 132	83 84	LOW END INPUT VOLTAGE RANGE 1 90V = 9000(×10mV) = 2328H STORED WITH LSB FIRST THEN MSB	40 35	28 23
133 134	85 86	HIGH END INPUT VOLTAGE RANGE 1 264V = 26400(×10mV) = 6720H STORED WITH LSB FIRST THEN MSB	32 103	20 67
135 136	87 88	LOW END INPUT VOLTAGE RANGE 2 0V = 0(×10mV) = 0H, no voltage range 2 STORED WITH LSB FIRST THEN MSB	00 00	00 00
137 138	89 8A	HIGH END INPUT VOLTAGE RANGE 2 0V = 0(×10mV) = 0H, no voltage range 2 STORED WITH LSB FIRST THEN MSB	00 00	00 00
139	8B	LOW END INPUT FREQUENCY RANGE, 47Hz = 2FH	47	2F
140	8C	HIGH END INPUT FREQUENCY RANGE, 63Hz = 3FH	63	3F
141	8D	A/C DROPOUT TOLERANCE IN ms, 12ms = 0CH	12	0C
142	8E	BINARY FLAGS 7-5: (000)b, reserved 4: (1)b, Tachometer Pulses per Rotation / Predictive Fail Polarity (2 Pulses Per Rotation = 1; 1 Pulse Per Rotation = 0) OR (Signal Asserted (1) Indicates Failure = 0, Signal De-asserted (0) Indicates Failure = 1) 3: (1)b, Hot Swap / Redundancy Support 2: (0)b, Auto Switch Support 1: (1)b, Power Factor Correction Support 0: (0)b, Predictive Fail Support	27	18
143 144 145	8F 90 91	Peak Wattage Capacity and Holdup Time 15-12: (0000)b, 12 mSeconds = 0CH 11-0: (1001011000)b, 760Watts = 0258H Stored with LSB first then MSB.	12 248 002	0C F8 02
146 147	92 93	Combined Wattage NOT APPLICABLE	00 00	00 00

OFFSET		DEFINITION	SPEC	VALUE
(DEC)	(HEX)	(REMARKS)	(DEC)	(HEX)
148	94	PREDICTIVE FAIL TACHOMETER LOWER THRESHOLD Not applicable	00	00
		12V DC OUTPUT RECORD HEADER		
149	95	RECORD TYPE ID (0X01 = DC OUPUT)	001	01
150	96	End of List/Record Format Version Number 7: (0)b, End of List 6-4: (000)b, reserved 3-0: (0010)b, record format version	002	02
151	97	Record Length: 13 Bytes	13	0D
152	98	Record Checksum (Zero Checksum From 154d to 166d)	83	53
153	99	Header Checksum (Zero Checksum From 149d to 152d)	157	9D
		+12V DC OUTPUT RECORD		
164	9A	+12V Output Information 7: (0)b, standby 6-4: (000)b, reserved 3-0: (0001)b, output number 1 = 001b	001	01
		NOMINAL VOLTAGE		
155 156	9B 9C	12.00V = 1200 (x10mV) = 04B0H Stored with LSB first then MSB.	176 004	B0 04
157 158	9D 9E	Maximum Negative Voltage Deviation 11.88V = 1188 (x10mV) = 04A4H. Stored with LSB first then MSB.	164 004	A4 04
159 160	9F A0	Maximum Positive Voltage Deviation 12.12V = 1212 (x10mV) = 04BCH Stored with LSB first then MSB.	188 004	BC 04
161 162	A1 A2	Ripple And Noise pk-pk 10Hz to 30MHz (mV) 100mV = 0064H Stored with LSB first then MSB.	100 000	64 00
163 164	A3 A4	Minimum Current Draw (10mA) 5.0A = 500 (x10mA) = 01F4H Stored with LSB first then MSB.	244 001	F4 01
165 166	A5 A6	Maximum Current Draw (10mA) 49.0A = 4900 (x10mA) = 1324H Stored with LSB first then MSB.	036 019	24 13
		5V0SB DC OUTPUT RECORD HEADER		
167	A7	Record Type ID (0x01 = DC Output)	001	01
168	A8	End of List/Record Format Version Number 7: (1)b, end of list 6-4: (000)b, reserved 3-0: (0010)b, record format version	130	82
169	A9	Record Length: 20 Bytes	020	14
170	AA	Record Checksum (Zero Checksum From 172d to 191d)	074	4A
171	AB	Header Checksum (Zero Checksum From 167d to 170d)	031	1F
		5V0SB DC OUTPUT RECORD		
172	AC	5V0SB Output Information 7: (1)b, Standby (Bit = 1 to indicate standby output) 6-4: (000)b, reserved 3-0: (0010)b, output number 2 = 010b	130	82
173 174	AD AE	Nominal Voltage 5.00V = 500 (x10mV) = 01F4H Stored with LSB first then MSB.	244 001	F4 01



OFF	SET	DEFINITION	SPEC	VALUE
(DEC)	(HEX)	(REMARKS)	(DEC)	(HEX)
175 176	AF B0	Maximum Negative Voltage Deviation 5.25V = 525 (x10mV) = 020DH Stored with LSB first then MSB.	013 002	0D 02
177 178	B1 B2	Maximum Positive Voltage Deviation 4.75V = 475 (x10mV) = 01DBH Stored with LSB first then MSB.	219 001	DB 01
179 180	B3 B4	Ripple And Noise pk-pk 10Hz to 30MHz (mV) 100mV = 0064H Stored with LSB first then MSB.	100 000	64 00
181	B5	Minimum Current Draw (10mA) 000 = 0000H	000	00
182	B6	Stored with LSB first then MSB.	000	00
183 184	B7 B8	Maximum Current Draw (10mA) 2.40A = 240(x 10mA) = 00F0H Stored with LSB first then MSB.	240 000	F0 00
185	В9	Reserved	00	00
186	ВА	Reserved	00	00
187	BB	Reserved	00	00
188	ВС	Reserved	00	00
189	BD	Reserved	00	00
190	BE	Reserved	00	00
191	BF	Reserved	00	00
		INTERNAL USE AREA, 64 bytes		
192	C0	Format Version Number 7:4 -reserved, write as 0000b 3:0 -format version number = 1h for this specification.	001	01
193 194 195 196 197 198 199 200 201 202 203 204 205 206 207 208 209 210 211 212 213 214 215 216 217 218 219 220	C1 C2 C3 C4 C5 C6 C7 C8 C9 CA CB CC CD CE CF D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 DA DB DC			00 00 00 00 00 00 00 00 00 00 00 00 00



OFF	SET	DEFINITION	SPEC	VALUE
(DEC)	(HEX)	(REMARKS)	(DEC)	(HEX)
221	DD		0	00
222	DE		0	00
223	DF		0	00
224	E0		0	00
225	E1		0	00
226	E2		0	00
227	E3		0	00
228	E4		0	00
229	E5		0	00
230	E6		0	00
231	E7		0	00
232	E8		0	00
233	E9		0	00
234	EA		0	00
235	EB		0	00
236	EC		0	00
237	ED		0	00
238	EE		0	00
239	EF		0	00
240	F0		0	00
241	F1		0	00
242	F2		0	00
243	F3		0	00
244	F4		0	00
245	F5		0	00
246	F6		0	00
247	F7		0	00
248	F8		0	00
249	F9		0	00
250	FA		0	00
251	FB		0	00
252	FC		0	00
253	FD		0	00
254	FE		0	00
255	FF	CHECKSUM: (From 192 to 254 if used)	PER	UNIT



The power supply will have a Power Supply Management Interface (PSMI) compliant with design guide V2.12. PSMI is a register based interface with an access protocol as shown in the diagrams below.

For format details and contents refer the PSMI design guide. Any registers not specified will return 0x00.

READ Protocol

s	Slave Addr	V A	Register number	Α	s	Slave Addr	R	Α	Low order data byte	Α	High order data byte	Α	Р	
---	---------------	-----	--------------------	---	---	---------------	---	---	---------------------	---	----------------------	---	---	--

WRITE Protocol

S	Slave Addr	w	Α	Register number	Α	Low order data byte	Α	High order data byte	Α	Р	
---	---------------	---	---	--------------------	---	---------------------	---	-------------------------	---	---	--

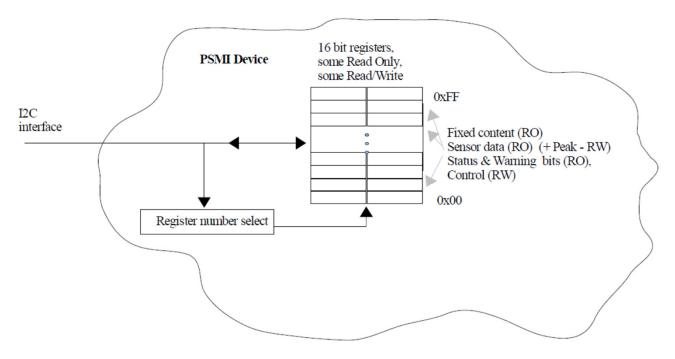
S = Start condition

P = Stop condition

W = Write

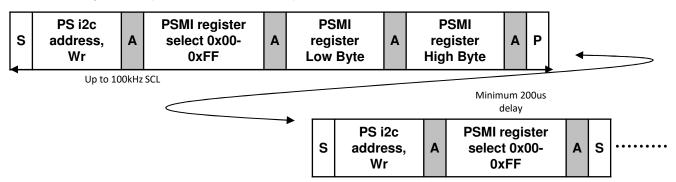
R = Read

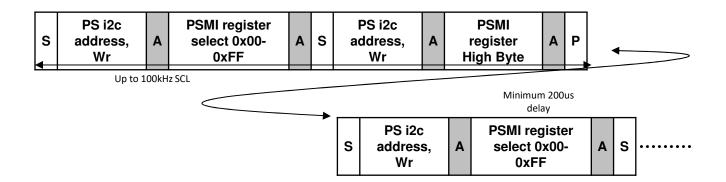
A = Acknowledge





Write to PSMI register, no repeated address, without stop





S: Start condition

P: Stop condition

A: Acknowledge

N: Not Acknowledge

Grey: driven by power supply



Register Definition

PSMI Regis	ter Address	Register Groups
0x00	0x05	Sensor (Temperature)
0x06	0x1F	PSMI Capability
0x20	0x23	Sensor (Fan Speed)
0x24	0x27	Control (Fan Speed)
0x28	0x32	Sensor (Voltage)
0x33	0x3D	Sensor (Current)
0x3E	0x52	PSMI Header
0x53	0x5D	Sensor (Peak Current)
0x5E	-	Shutdown
0x5F	0x61	Warning
0x62	-	Status
0x63	-	Control
0x64	0xBF	PS Capability Records
0xC0	0xDF	Custom Registers
0xE0	0xFF	PS Capability Records (2)



PSMI Header

The PSMI device shall include the discovery key ("PSMI"), PSMI specification revision number, power supply code revision, and optionally LANA Enterprise ID. All registers are read only.

Register Number	Name	Register D	Description
Register Number	ivaille	Bits 0 - 7	Bits 8 - F
0x3E	Discovery key 1-2	"P"	"S"
0x3F	Discovery key 3-4	"M"	" "
0x40	PSMI version	Major version 0x02	Minor version 0x12
0x41	PSU code version	Major version to be defined by supplier	Minor version to be defined by supplier
0x42	Supplier ID	Reserved for LANA Enterprise ID LS	Reserved for LANA Enterprise ID
0x43	Supplier ID 2	Reserved for LANA Enterprise ID	Reserved for LANA Enterprise ID
0x44 - 0x52	Reserved	0x0000	



PSMI Sensors

Dogistor Number	Nama	Register Description	
Register Number	Name	Bits 0 - 7 Bits 8 - F	
0x06	Thermal sensor configuration	To be defined by supplier. Expected to be 1 fan sensor, 1 temperature sens association between sensors and fans.	sor no
0x07	Temperature sensor types	To be defined by supplier. Expected to be internal.	
0x08	T1 temperature sensor offset	Not present, 0x0000.	
0x09 - 0x0B	T2, T3, T4 temperature sensor offset	Not present, 0x0000.	
0x0C	Fan 1, 2 resolution register	Not present, 0x0000.	
0x0D	Fan 3, 4 resolution register	Not present, 0x0000.	
0×0E	F1 config	0x3E80	
0x0F - 0x11	F2, F3, F4 config	Not present, 0x0000.	
0x12	Voltage / Current sensor configuration.	0x0E32. 2 outputs, 2 output voltage sensor, 1 output current sensor, input v sensor, input current sensor, peak current sensor.	voltage
0x13	Fan associations	0x0000	
0x14	F1, F2 cont	0x0000	
0x15	F3, F4 cont	0x0000	
0x16	Shutdown events register capability	0x001F	
0x17	Status capability	0x0071	
0x18	Control / Record capability	0x0111	
0x19	Warning events capability	0x1891	
0x1A - 0x1F	Reserved	0×0000	



Sensor data shall be updated at least once every 250ms for temperatures, currents and voltages. Fan data shall be updated at least once a second. Data representation shall be 16 bits however the sensor resolution shall be 8 bits or greater were specified and placed into the 16 bits format as individually defined below.

• Temperature sensor data shall be relative to a target defined in the PS capability section. The actual temperature is the value from the register plus the offset defined in the PSMI capabilities section (register 0x08).

Sensor	Range	Resolution	Register	Error
Relative temperature to T1 target in PSMI capability	-20°C~+15°C	0.25 ^o C	0x00	+/-1°C over range from - 20°C to +15°C from target temperature

М	SB Upper nibble MSB Lower nibble							LS	SB Upp	er nibb	le		L	SB Low	er nibb	le		
X	Χ	Χ	X		Χ	X	Χ	Х		Χ	X	Χ	Χ		Χ	Χ	Χ	Χ
Sign		Integer value (0-511)											F	raction	al value	(1/640	2)	

Fan rotation in RPM shall be available.

Sensor	Range	Resolution	Register	Error
F1 Sensor	0 - 65635RPM	TBD	0x20	TBD

	MSB Upper nibble MSB Lower nibble							L;	SB Upp	er nibb	le	LSB Lower nibble					
X	X	X	X		Χ	Χ	Х	Χ		Х	Χ	X	X	Χ	Χ	Χ	Χ
							lr	nteger v	alue (0	- 65535	5)						

• Output current for V1 shall be measured and represented as below.

Sensor	Range	Resolution	Register	Error
V1 Current	0 - 1024A	0.34A	0x33 Peak in 0x53	+/-5% Rated Current

The peak register shall be reset at power on or if the peak register is written to

N	MSB Upper nibble MSB Lower nibble						le		LSB Upper nibble LSB I						SB Low	ower nibble		
X	Χ	Χ	Χ		Χ	X X X X				Х	Χ	Х	Χ		Χ	Χ	Χ	Χ
Integer value (0 - 1023)											Fr	actiona	l value	(1 / 64	4)			



Input current for the power supply shall be measured and represented as below

Sensor	Range	Resolution	Register	Error
Input Current	0 - 1024A RMS	0.06A	0x3D Peak in 0x5D	+/-5% Rated Current

N	MSB Upper nibble MSB Lower nibble						LSB Upper nibble					LSB Lower nibble					
X	Х	Х	Х		Х	Х	Х	Х	Х	Χ	Х	Χ		Х	Χ	Х	Χ
	Integer value (0 - 1023)										Fr	actiona	al value	(1 / 64	4)		

The peak register shall be reset at power on or if the peak register is written to.

The input current register value (not peak register) shall be averaged over at least 2 seconds.

Input voltage for the power supply shall be measured and represented as below.

Sensor	Range	Resolution	Register	Error
Input Voltage	0 - 320VAC RMS	1.26VAC	0x32 (RO)	+/-5% Rated Voltage

M	ISB Upp	er nibb	le		М	SB Low	er nibb	le		LS	SB Upp	er nibb	le		LSB Lower nibble				
X	Χ	Х	Χ		Χ	X X X X				Χ	X	X	X		Χ	X	Χ	Х	
Sign		Integer value (0 - 1023)												Fract	ional va	lue (1 /	32V)		

Note the sign is always 0 (positive) for the AC RMS input.

• Output voltage for the power supply shall be measured and represented as below.

Sensor	Range	Resolution	Register	Error
Output Voltage	+/-128V	1/190 rated voltage	0x28 (RO)	+/-2%

M	ISB Upp	er nibb	le		М	SB Low	er nibb	ole	LSB Upper nibble			L	SB Low	er nibb	le		
X	Χ	Χ	Х		Х	Χ	Х	Х	Χ	X	X	Χ		Χ	Χ	Χ	Χ
Sign	Integer value (0 - 127)							Fra	actiona	l value (1 / 256	iV)					



Danista Novebar	Nama	Register D	escription
Register Number	Name	Bits 0 - 7	Bits 8 - F
0x00	T1 temperature	Relative temperature to T1 target	
0x01 - 0x05	T2, T3, T4 reserved	Not used 0x0000	
0x20	F1 sense	F1 speed in RPM	
0x21 - 0x23	F2, F3, F4 sense	Not used 0x0000	
0x28	V1 output voltage	V1 output voltage	
0x29 - 0x31	V2 - V10 output voltage	Not used 0x0000	
0x32	Input voltage	Input voltage	
0x33	V1 output current	V1 output current	
0x34 - 0x3C		Not used 0x0000	
0x3D	Input current	Input current	
0x53	V1 output current Peak	V1 peak output current Read / Write	
0x54 - 0x5C		Not used 0x0000 Read / Write	
0x5D	Input current Peak	Peak input current Read / Write	



PSMI Shutdown

The power supply shall provide a shutdown event register (0x5E, R/W) which will maintain data while the standby rail is present even if the AC supply to the power supply is lost. The register will be cleared at initial power on, when PSON is cycled, and if 1 is written to the associated bit.

Shutdown register 0x5E bit	Name	Detail
0	Failure	1 - if the power supply not supplying output due to internal shutdown including over current, over temperature, over or under voltage, fan failure, device failure. Also AC failure 0 - if no faults
1	Over Current	1 - if any output has over current (note 5.0Vstby must still power the interface) 0 - if normal operation
2	Over Temperature	1 - if PS shutdown due to over temperature 0 - if normal operation
3	AC Loss	1 - if PS shutdown for AC loss, not asserted for momentary loss of AC where PS does not shutdown 0 - for normal operation
4	Fan Failure	1 - if PS shutdown due to fan failure 0 - if normal operation
5 - F	Reserved	Must return 0



PSMI Warning

The power supply shall provide shutdown event register for thermal warnings, output over current warnings, and input warnings (0x5F, 0x60, 0x61, R/W) which will maintain data while the standby rail is present even if the AC supply to the power supply is lost. The register will be cleared at initial power on, when PSON is cycled, and if 1 is written to the associated bit.

Thermal warning register 0x5F bit	Name	Detail
0	T1 cont warning	1 - if the power supply temperature has exceeded the maximum value in the PS capabilities registers 0 - if not exceeded the temperature
1 - 3	Not used	Must return 0
4	F1 warning	1 - if fan failure is predicted 0 - if normal operation
5 - F	Not used or reserved	Must return 0

Current warning register 0x60 bit	Name	Detail
0	V1 current warning	1 - if the power supply output on V1 has exceeded the maximum value in the PS capabilities registers 0 - if not exceeded the current limit
1 - F	Not used	Must return 0

Input warning register 0x61 bit	Name	Detail
0	Input over current warning	 1 - if the power supply input current has exceeded the maximum value in the PS capabilities register 0 - if not exceeded the current limit
1 - 2	Not used	Must return 0
3	Input under voltage warning	1 - if the power supply input voltage was below the minimum value in the PS capabilities register 0 - if not dropped below the minimum input voltage limit
4 - F	Not used	Must return 0



PSMI Status

The power supply shall provide a status register which will maintain data while the standby rail is present even if the AC supply to the power supply is lost. The register will be cleared at initial power on and when PSON is asserted.

Status register 0x62 bit	Name	Detail
0 RO	RPMI over-ride	1 - if fan speed over-ride is in operation0 - if fan speed over-ride is not in operation
1 - 3 RO	Not used	Must return 0
4 RO	PW_OK	1 - if the power supply PW_OK is asserted 0 - if the power supply PW_OK is not asserted
5 RO	PSON/L	1 - if the PSON/L signal to the power supply is asserted 0 - if the PSON/L signal to the power supply is not asserted
6 R/W	SMB_ALERT/L	1 - if the power supply SMB_ALERT/L interrupt to the system is asserted, caused by an event and latched on. 0 - if the power supply SMB_ALERT/L is not asserted This bit shall be reset to 0 by power cycle or writing 1 to this register bit
7, 8 RO	Power supply operating range	Input operating range - It has only one range so always 00b
9 RO	Redundancy	Must return 0 - only used on PDB
A - F RO	Not used	Must return 0



PSMI Control

The power supply shall provide registers for fan speed control and miscellaneous control items, the miscellaneous control register shall be reset on initial power on and maintain values whenever 5V standby is present.

Fan speed Control register 0x24 bit	Name	Detail
0 - 7	F1 cont	Fan speed increase function shall be available with the control represented as an 8 bits number giving the % duty cycle for the PWM $(0 = 0\%, 255 = 100\%)$
8 - E	Not used	Must return 0

Register Number	Name	Register Description			
Register Number	Ivaille	Bits 0 - 7	Bits 8 - F		
0x25 - 0x27	F2, F3, F4 speed control	Not used 0x0000			

Control register 0x63 bit	Name	Detail
0	RPMI over-ride	1 - if fan speed over-ride is in operation 0 - if fan speed over-ride is not in operation
1 - 3	Not used	Must return 0
4	Shutdown LED status	1 - if shutdown LED is turned on by the system 0 - if controlled by the power supply (Default) This will turn on the Amber Fail LED. Note either shutdown or warning LED control shall turn that LED on Amber
5	Warning LED status	1 - if warning LED is turned on by the system 0 - if controlled by the power supply (Default)
6	Shutdown event mask	1 - if shutdown events cause an interrupt (Default) 0 - if shutdown events do not cause an interrupt
7	Warning event mask	1 - if warning events cause an interrupt (Default) 0 - if warning events do not cause an interrupt
8 - F	Reserved	Must return 0



PSMI Power Supply Capability Records

The power supply shall implement the registers in the table below, other registers within the power supply capabilities. Records are not used and shall return 0 if read. All registers in this section are defined as read only. Data formats are defined in the PSMI design guide.

	,,	Register Description				
Register Number	Name	Bits 0 - 7	Bits 8 - F			
0x64	T1 target	Defined by suppliers, operating temperature of T1 sensor, must be lower than shutdown limit.				
0x65 - 0x67	T2, 3, 4 target	Not used 0x0000				
0x68	F1 min	Defined by supplier, minimum fan speed in F	RPM (0 - 65535RPM)			
0x69 - 0x6B	F2, 3, 4 min	Not used 0x0000				
0x6C	Fan sound	0x00 max	0x00 min			
0x6D	V1 output max voltage	From regulation specification				
0x6E	V1 output min voltage	From regulation specification				
0x6F	Vsb output max voltage	From regulation specification				
0x70	Vsb output min voltage	From regulation specification				
0x71 - 0x80	Vout 3-10 limits	Not used 0x0000				
0x81	lout1 @ V-input R1	Set to 62.3A for DS760SL-3; Set to 49.0A for DS760SL-3-001				
0x82	lout2 @ V-input R1	Set to 2.4A				
0x83 - 0x84	lout 3-10 @ V-input R1	Not used 0x0000				
0x8B - 0x94	lout 1-10 @ V-input R2	Not used 0x0000				
0x95 - 0x9E	lout 1-10 @ V-input R3	Not used 0x0000				
0x9F	First input current limit	Defined by supplier as maximum rated input	current at 90VAC			
0xA0	Second input current limit	Not used 0x0000				
0xA1	Third input current limit	Not used 0x0000				
0xA2	First input voltage min	Set to 90VAC				
0xA3	Second input voltage min	Not used 0x0000				
0xA4	Third input voltage min	Not used 0x0000				
0xA5	First output power limit	Set to 760W for DS760SL-3; Set to 600W for DS7690SL-3-001				



Danistas Novebra	Nama	Register Description	
Register Number	Name	Bits 0 - 7	Bits 8 - F
0xA6	First output power limit	Not used 0x0000	
0xA7	First output power limit	Not used 0x0000	
0xA8	Combined output power limit1	0x0000 no combined limit	
0xA9	Combined outputs for power limit1	0x0000 no combined limit	
0xAA	Combined output power limit2	0x0000 no combined limit	
0xAB	Combined outputs for power limit2	0x0000 no combined limit	
0xAC	Output1 current sensor bandwidth	Defined by supplier	
0xAD	Input current sensor bandwidth	Defined by supplier	
0xAE	High line light load output power	STS #7	
0xAF	High line mid-load output power	STS #6	
0xB0	High line max load output power	STC #3	
0xB1	High line efficiency1	High line light load efficiency. Defined by supplier. The efficiency data is returned as an 8-bit binary value with each 1 bit increment representing (1/256%)	High line mid load efficiency. Defined by supplier.
0xB2	High line efficiency2	High line max load efficiency. Defined by supplier.	0x00
0xB3	Low line light load output power	STC # 5	
0xB4	Low line mid-load output power	STS #4	
0xB5	Low line max load output power	STC #2	
0xB6	Low line efficiency1	Low line light load efficiency. Defined by supplier. The efficiency data is returned as an 8-bit binary value with each 1 bit increment representing (1/256%)	Low line mid load efficiency. Defined by supplier.
0xB7	Low line efficiency2	Low line max load efficiency Defined by supplier	0x00
0xB8	V1 (12V) load share accuracy	To be defined by supplier (must be 5.4A or better) represented as a range 0 to 25.5A in 0.1A increments	0x00



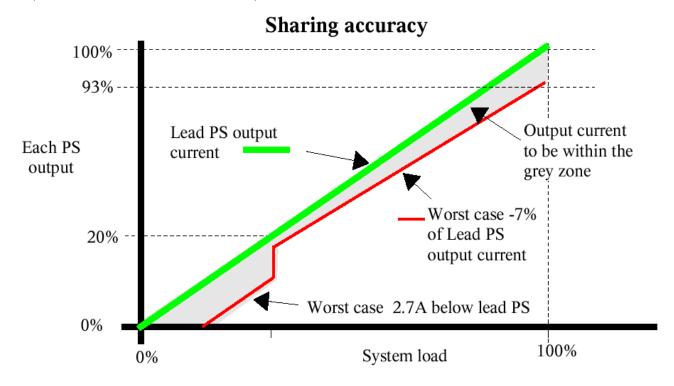
Dogistor Number	Name	Register Description	
Register Number		Bits 0 - 7	Bits 8 - F
0xB8 - 0xBB	V2, V3, V4 load share accuracy	Not used 0x0000	0x00
0xBC	Redundancy configuration	Not used 0x0000 (PDB use only)	
0xBD - 0xBF	Not used	Not used 0x0000	
0xE0 - 0xFF	Not used	Not used 0x0000	



APPLICATION NOTES

Current Sharing

The DS760SL series' main output is equipped with current sharing capability. This will allow up to 4 power supplies to be connected in parallel for higher power application. All outputs with active current sharing will share load current within 10% of the average current at operating load. This will be valid for all loads greater than 20% rated output. For loads less than 20% of rated output the share will be 5% of the full rated output.



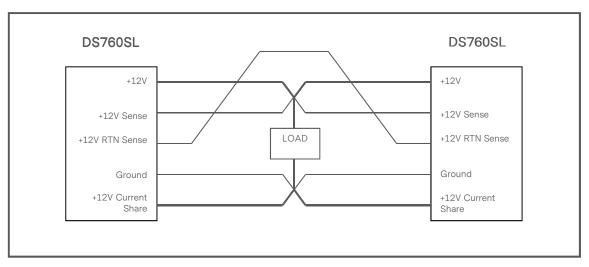
All outputs with active current sharing will share load current within 10% of the average current at operating load. This shall be valid for all loads greater than 20% rated output. For loads less than 20% of rated output the share shall be 5% of the full rated output.



APPLICATION NOTES

Redundancy / Fault Tolerance

The DS760SL series power supplies can be connected in the following to provide redundancy/fault tolerance operation:



The main output will be capable of operating in a redundant current share mode. A maximum of 4 power supplies may be operated in parallel. All outputs will incorporate an isolation device for fault isolation. Filter capacitors that are located after the isolation device will be of high reliability and will be de-rated sufficiently to minimize failures.

Outputs of two (or more) supplies connected in parallel must meet the regulation requirements of a single supply. Under normal operation with two (or more) supplies running in parallel the outputs must share load current. If one of the supplies fails the remaining supply (supplies) must pick up the entire load without causing the output to go out of regulation. A defective supply that is connected to the output voltage bus will cause no adverse effect on bus or the operation of the remaining functional supply (supplies).

When the parallel units operate within the specified input, output conditions, power up and power down conditions the power supplies will not exhibit any instability. The bus voltage will be within the regulation band, and the bus's periodic and random deviation will meet individual differential supply specification requirements. At initial start-up the load will be limited to the rating of one power supply.

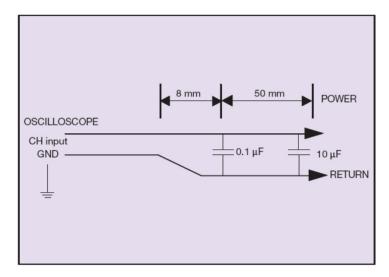
Output	Voltage (V)	For N power supplies in parallel combined current (A)	Load step current (A)	
Vo	12.0	2 PS - 118.37	31.2	
V_{SB}	5.0	2 PS - 4	1.2	



APPLICATION NOTES

Output Ripple and Noise Measurement

The setup outlined in the diagram below has been used for output voltage ripple and noise measurements on the DS760SL series. When measuring output ripple and noise, a scope jack in parallel with a 0.1uF ceramic chip capacitor, and a 10uF aluminum electrolytic capacitor should be used. Oscilloscope should be set to 20MHz bandwidth for this measurement.





RECORD OF REVISION AND CHANGES

Issue	Date	Description	Originators
1.0	08.09.2010	First issue	A. Fu
1.1	08.20.2013	Update to the Artesyn template	A. Fu
1.2	09.11.2014	Update the typo error	A. Fu
1.3	07.08.2016	Update the system timing	A. Fu
1.4	03.04.2019	Update PSU output voltage PSMI specification	E. Wang
1.5	03.03.2021	Update cover and back cover	C. Liu





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