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1. SCOPE

This document specifies the communication interface features and limitations of DS2000SPE-3 PSU. Each PMBus™ command is not discussed in this document. Only commands with notable implementation details are discussed. The PMBus specification document must be used for general PMBus definitions.

2. REFERENCES

2.1. Applicable Documents

Document	Revision
System Management Bus (SMBus) Specification http://smbus.org/specs/	2.0
PMBus ™ Power System Management Protocol Specification Part II – Command Language http://pmbus.org/specs.html	1.2

3. DEFINITIONS

3.1. Abbreviations and Acronyms

Term	Definition
PMBus	Power System Management Bus
I2C	Inter-integrated circuit
SMBus	System Management Bus
MCU	Microcontroller
EEPROM	Electrically Erasable Programmable Read-Only Memory
SDA	Serial data signal (bi-directional)
SCL	Serial clock signal
NACK	Not Acknowledge (an I2C signaling indicating a byte error)
PSU	Power Supply Unit

4. GENERAL CHARACTERISTICS

4.1. Clock Frequency

Only standard mode operating frequency of 10 KHz to 100 KHz is supported.

4.2. Device Addressing

Slave device address is configurable via address pins. Base address is 0xB0. Below is the table of the possible addresses that can be used via the address pin configuration. Note that the address pins are in high state initially.

ADDRESS PINS			PMBUS WRITE ADDRESS	PMBUS READ ADDRESS
A2	A1	A0		
1	1	1	0xBE	0xBF
1	1	0	0xBC	0xBD
1	0	1	0xBA	0xBB
1	0	0	0xB8	0xB9
0	1	1	0xB6	0xB7
0	1	0	0xB4	0xB5
0	0	1	0xB2	0xB3
0	0	0	0XB0	0XB1

4.3. Transaction Interval

The recommended minimum regular interval between transactions is 15msec.

4.4. Timeouts

Internal timeouts are implemented to prevent bus lock up.

4.4.1. Transaction Timeout

If a transaction is not completed and the interface remains quiet for 80msec, a transaction timeout will occur. The timeout will cause the internal state machine of the PMBus interface to reset. This transaction timeout is particularly useful for systems with multi masters. In case a master device fails in the middle of a transaction, this timeout enables the PSU to be ready to accept another transaction from another master.

4.5. Packet Error Checking (PEC)

The PSU complies with PEC as specified in the SMBus specification. A master device may communicate with the PSU with our without PEC. However, it is highly recommended to always use PEC to avoid reading or writing incorrect data due to possible noise in the bus.
The PEC byte in any transaction will be acknowledged (ACK) by the PSU whether the PEC validation is successful or not. The response of the PSU for unsuccessful validation is discussed in section 4.8 Error Handling.

4.6. Data Format

Refer to section 10.1 Commands List Summary.

4.7. Alert

An alert signal is used to indicate that a fault occurred. This signal conforms to the SMBAlert# specification, except the part about acknowledging the Alert Response Address. It is de-asserted using the CLEAR FAULT command instead.

Refer to product pin out specifications for the pin used as SMBALERT#.

4.8. Error Handling

4.8.1. Communication Errors

The STATUS_CML command indicates occurrences of PMBus communications errors.

- Invalid or Unsupported Command Received
  - A PMBus command code was received that is not included in the supported commands of the product.
  - A write operation on a PMBus command code which is under the Basic Write Protection, but the present WRITE_PROTECT value prohibits writing to the PMBus command.
  - If a read operation is performed on an unsupported command, the data that will be returned by the PSU shall be all 0xFF as long as the host keeps on clocking out data.
  - A write operation on a read-only command
  - A read on a command using Send Byte transaction type.
  - If PEC is used in the transaction, the PEC validation should be successful. Otherwise, PEC error will take the higher priority.
  - Assertion of this flag shall not consider whether the command is for internal use only or not.
  - STORE_USER_ALL request during bulk bad
- Invalid or Unsupported Data Received
  - Some PMBus commands may specify a valid data range it can accept. This will vary from product to product and shall be specified in the product documentation. If the data written to the command is not within the valid range, this event will be triggered.
  - If byte count used on block write operation is greater than the value defined in the product specification, this event shall be triggered.
  - If PEC is used in the transaction, the PEC validation should be successful. Otherwise, PEC error will take the higher priority.
- Packet Error
  - A transaction use PEC and the PEC validation was not successful. Even if the command code received is not part of the supported commands or the data received is not within the valid range, as long as there is PEC error, only the Packet Error event shall be triggered.

4.9. Write Protection

There are two levels of write protection that prevents unintentionally overwriting writeable commands: (1) Basic Write Protection; (2) Configuration Mode Write Protection.
Written data to any command will only be saved in the non-volatile memory if a “save” command is issued. Each protection mode shall have its own command to be able to save the configuration written to registers under it.

4.9.1. Basic Write Protection

The basic write protection is equivalent to the PMBus command WRITE_PROTECT (command code 10h). The default value of this command is be 80h, which means all writes are disabled except a write to the WRITE_PROTECT command itself. This command code shall support a read/write byte transaction type; however, the value written to it shall not be stored to non-volatile memory. This means that every time the product restarts the WRITE_PROTECT always reverts to the default value even if the write protection has been disabled prior to the restart.

Values written to writeable command codes under the Basic Write Protection is only stored in the non-volatile memory using the PMBus command STORE_USER_ALL. If the STORE_USER_ALL command is not issued, the new values written will revert to the original value once the PSU goes through a hard restart (input supply is removed until all internal bias is lost). Note that the STORE_USER_ALL command is under Configuration Mode Write Protection.

4.9.2. Configuration Mode Write Protection

The configuration mode write protection covers all command codes that are critical to the power supply operation, which requires a tighter change control.

These command codes shall include:

- Saving user configurable parameters
- Calibration data
- Critical product configuration data
- Manufacturing information data
- FRU data

Values of all writeable command codes under the Configuration Mode Write Protection will only be stored in the non-volatile memory using the PMBus command STORE_USER_ALL. Refer to the PMBus Command Codes Matrix for details on command codes used and which commands are under the Configuration Mode Write Protection.

5. OPERATING MODES

There shall be three operating modes with respect to how a system may communicate (monitor, configure, reprogram) the PSU: (1) MAP Mode, (2) Configuration Mode, and (3) ISP Mode.

5.1. MAP Mode

The MAP (Main Application Program) Mode is the normal operating mode of the PSU. In this mode, readable parameters are available. However, only commands under the Basic Write Protection Mode can be written. New values written to any command in MAP mode are volatile (values will be reset to original if power is recycled).

5.2. Configuration Mode

To enable writing to commands under Configuration Mode Write Protection, the PSU must enter Configuration Mode. There are two classification of Configuration Mode:

5.2.1. User Configuration Mode

Certain configurable parameters such as warning limits and fault limits can only be overwritten when PSU is in User Configuration Mode.
This mode is intended for user systems to modify critical parameters of the PSU while maintaining restriction for unintentional overwrite.

5.2.2. Factory Configuration Mode

This mode is for configurations that are intended to be used only in a controlled environment (e.g. Factory, Value Added Resellers), and done by qualified personnel. These configurations include critical parameters such as Calibration Registers.

5.3. ISP Mode

In ISP (In-System Programming) Mode, the firmware can be updated through the PMBus communication interface. Both the MAP and Configuration Mode functions are inhibited in ISP Mode with the exception of some PMBus commands related to the ISP operation. Only the MAP firmware will be affected by any firmware update in ISP mode. All data of PMBus (except those that should change along with a firmware update, e.g. FW version) and configuration registered in the non-volatile memory will not be altered in ISP mode.
In case of a problem during firmware update (e.g. loss of power, communication error, corrupted MAP firmware, etc.) the product will remain or boot up in ISP mode to be able to reinitiate and complete the firmware update process. After a successful firmware update the PSU shall operate normally again.

6. BITMAPPED REGISTERS

6.1. Status Registers

This section specifies the PMBUs status bits that are supported in the different status registers.
Note: ✓ - Supported bit, _ - Not Supported bit

6.1.1. STATUS_BYTE and STATUS_WORD

Byte	Bit #	Status Bit Name	Supported Bits	Remarks
Low Byte (STATUS_BYTE)	7	BUSY		
	6	OFF	✓	
	5	VOUT_OV_FAULT	✓	
	4	IOUT_OC_FAULT	✓	
	3	VIN_UV_FAULT	✓	
	2	TEMPERATURE	✓	
	1	CML	✓	
	0	NONE OF THE ABOVE		
High Byte	7	VOUT	✓	
	6	IOUT/POUT	✓	
	5	INPUT	✓	
	4	MFR_SPECIFIC		
	3	POWER_GOOD#	✓	
	2	FANS	✓	Will not set due to Fan Override
	1	OTHERS		
	0	UNKNOWN		

6.1.2. STATUS_VOUT

Bit #	Status Bit Name	Supported Bits	Remarks
7	VOUT_OV_FAULT	✓	
6	VOUT_OV_WARNING	✓	
5	VOUT_UV_WARNING	✓	
4	VOUT_UV_FAULT	✓	
3	VOUT_MAX Warning		
2	TON_MAX_FAULT	✓	
1	TOFF_MAX_WARNING		
0	VOUT Tracking Error		

6.1.3. STATUS_IOUT

Bit #	Status Bit Name	Supported Bits	Remarks
7	IOUT_OC_FAULT	✓	
6	IOUT_OC_LV_FAULT		
5	IOUT_OC_WARNING	✓	
4	IOUT_UC_FAULT		
3	Current Share Fault		
2	In Power Limiting Mode		
1	POUT_OP_FAULT		
0	POUT_OP_WARNING	✓	

6.1.4. STATUS_INPUT

Bit #	Status Bit Name	Supported Bits	Remarks
7	VIN_OV_FAULT		
6	VIN_OV_WARNING	✓	
5	VIN_UV_WARNING	✓	
4	VIN_UV_FAULT	✓	
3	Unit Off For Insufficient Input Voltage	✓	Absence of or no input condition (not UV)
2	IIN_OC_FAULT		
1	IIN_OC_WARNING		
0	PIN_OP_WARNING		

6.1.5. STATUS_TEMPERATURE

Bit #	Status Bit Name	Supported Bits	Remarks
7	OT_FAULT	✓	
6	OT_WARNING	✓	
5	UT_WARNING		
4	UT_FAULT		
3	Reserved		
2	Reserved		
1	Reserved		
0	Reserved		

6.1.6. STATUS_CML

Bit #	Status Bit Name	Supported Bits	Remarks
7	Invalid Or Unsupported Command Received	✓	The following conditions shall also assert this flag: - A write transaction on read only commands - A write transaction on a password protected command that is still locked
6	Invalid Or Unsupported Data Received	✓	
5	Packet Error Check Failed	✓	
4	Memory Fault Detected	✓	
3	Processor Fault Detected		
2	Reserved		
1	A communication fault other than the ones listed in this table has occurred		
0	Other Memory Or Logic Fault has occurred.		

6.1.7. STATUS_FANS_1_2

Bit #	Status Bit Name	Supported Bits	Remarks
7	Fan 1 Fault	✓	
6	Fan 2 Fault		
5	Fan 1 Warning	✓	
4	Fan 2 Warning		
3	Fan 1 Speed Overridden	✓	
2	Fan 2 Speed Overridden		
1	Airflow Fault		
0	Airflow Warning		

6.2. Output Control Registers

6.2.1. OPERATION

Bit #	Status Bit Name	Supported Bits	Remarks
7 - 6	7 - Unit ON 6 – Soft Off	✓	00 – INVALID INPUT 01 – PSU OFF 10 – PSU ON (Default) 11 – INVALID INPUT
5 - 4	5 – Margin High 4 – Margin Low		00 – VALID INPUT (Default)
3 - 2	3 – Margin Act on Fault 2 – Margin Ignore Fault		00 – VALID INPUT (Default)
1 - 0	Reserved		00 – VALID INPUT (Default)

6.2.2. ON/OFF CONFIG

Bit #	Status Bit Name	Supported Bits	Remarks
7 - 5	Reserved		00 – (Default)
4	Control Pin And Serial Communication Control	✓	1 – Unit powers up as dictated by CONTROL pin and OPERATION command
3	Serial Communication Control	✓	1 - Enables Serial communication ON/OFF portion of OPERATION command. Requires CONTROL pin to be asserted for the unit to start and energize the output.
2	Control Pin	✓	1 - Unit requires CONTROL pin to be asserted to start the unit.
1	Control Pin Polarity	✓	0 - Active Low(Pull Low to start the unit)
0	Control Pin Action	✓	0 - Use programmed turn ON/OFF delay

Note:
This command is read-only.
Control Pin is the PSON# input to PSU

7. MANUFACTURER SPECIFIC COMMANDS

This section describes the Manufacturer Specific Commands to be supported by the PSU.

Convention:

In the Illustrations provided in the following sections slave addresses B0h (write) and B1h (read) are used just for example purposes.

S = Start Condition, P = Stop Condition, A = Ack, N= Nack, Sr = Repeated Start

A block highlighted in gray, means a response coming from the slave device.

7.1. FW_PRI_VERSION and FW_SEC_VERSION

Command codes E0h and E1h are used for FW_PRI_VERSION and FW_SEC_VERSION respectively. These commands are used to retrieve the primary side and secondary side MAP firmware versions of the product. Block read protocol is used with an 8-byte data size in ASCII format.

S	Slave Addr / W	A	FW_PRI/SEC_VERSION Command Code	A	Sr	Slave Addr/ R	A	Byte Count = 8	A	...

M1	A	M2	A	'.'= 2Eh	A	m1	A	m2	A	'.'= 2Eh	A	t1	A	t2	A	PEC	N	P

Where:

M1M2: Major firmware revision

m1m2: Minor firmware revision

t1t2: Test/integration firmware revision

8. IN-SYSTEM FIRMWARE UPDATE

This section describes the different commands involved in the in-system programming (firmware update) and the process in performing the update.

8.1. ISP Related Commands

8.1.1. ISP_UNLOCK_CODE

The ISP_UNLOCK_CODE command (command code F1h) is used to enable the use of ISP_CTRL_CMD. By default, the ISP_CTRL_CMD is always disabled upon start up in Main Application Program (MAP) mode.

This command uses the block write/read protocol. To use the ISP_UNLOCK_CODE command, the ASCII equivalent of the string “Boot” should be written as data bytes. When unlocked, writing any string aside from “Boot” shall lock ISP again and disable the use of ISP_CTRL_CMD.

A read to this command will return all zero values.

Write:

S	Slave Addr / W	A	ISP_UNLOCK_CODE Command Code	A	Byte Count = 4	A

…

‘B’= 42h	A	‘o’= 6Fh	A	‘o’= 6Fh	A	‘t’= 74h	A	PEC	A	P

8.1.2. ISP_CTRL_CMD

The ISP_CTRL_CMD command (command code F2h) is used to control In-System Programming (ISP) operations depending on the operating mode of the PSU. This command uses the read/write byte protocol. Reading this command code returns the last data/command byte that has been written.

Data/Command Byte	Description	Applicability
00h	- Exit ISP mode - Attempt to boot the main application program	PSU in ISP mode
01h	- Enter ISP mode - Enable all commands required to perform an in-system firmware update	PSU in MAP mode
03h	- Restart programming sequence - Clear the following bits of ISP_CONFIG_STATUS: • bit 1 (Startup Error) • bit 3 (Boundary Error) • bit 4 (Packet Size Error) • Set bit 2 (Checksum Error) of ISP_CONFIG_STATUS • Reset the address counter to the start address indicated in section 0 If the current memory counter is set to the start address of MAP, writing a 16-byte data block will erase the entire MAP memory block that will be written with the new program. It is recommended that after writing the first 16-byte data block, wait for	PSU in ISP mode

	at least 2 seconds before sending the second 16-byte data block. Afterwards, data blocks can be sent continuously. • • Parsing the Firmware Image	

8.1.3. ISP_CONFIG_STATUS

The ISP_ CONFIG_STATUS (command code F3h) provides the firmware update and configuration (when in Configuration Mode) status. This is a read word command whose data shall be interpreted as follows:

Bit#	Description
0	Mode: 1 – PSU is in ISP mode 0 – PSU is in MAP mode
1	Startup Error 1 – Startup program memory integrity check error 0 – Successful startup program memory validation
2	Checksum Error 1 – Failed checksum validation of a completed firmware update 0 – Successful checksum validation
3	Boundary Error 1 – The host system tried to program more than the maximum writeable memory blocks 0 – No boundary error
4	Packet Size Error 1 – Maximum ISP packet size exceeded 0 – No Error
5	ISP Pass Code Error 1 – Incorrect ISP pass code was used 0 – No Error
6 - 15	These bits are reserved to indicate status related to configuration mode. The usage of these bits may vary per product until the standard is specified.

8.1.4. ISP_FLASH_DATA

The ISP_FLASH_DATA (command code F5h) is used to write/read a 16-byte block of data to/from the current flash address. This is a read/write block command. After every read or write using this command, the memory address counter shall increment automatically by 16.

The byte count of data to be written should always be 16 to maintain proper alignment. Otherwise, firmware update validation will fail.

If the current memory counter is set to the start address of MAP, writing a 16-byte data block will erase the entire MAP memory block that will be written with the new program. It is recommended that after writing the first 16-byte data block, wait for at least 2 seconds before sending the second 16-byte data block. Afterwards, data blocks can be sent continuously.

8.2. Parsing the Firmware Image

The firmware is in S-Record format. Since only the data words of the s-record are needed in the update process, the record must be parsed to remove the other parts that are not needed (e.g. record type, byte count, address, checksum).

In an S-record file, all records with record type S1, S2 and S3 will be used. These are called Data Sequence records. Other record types are discarded. All data sequence records starting from address **0000h** until **7000h** in the S-record file must be parsed and sent to the PSU contiguously in 16-byte groups.

Suppose a random line on the S file:

```
S3110000050054E1800554E1800554E2E4302B
```

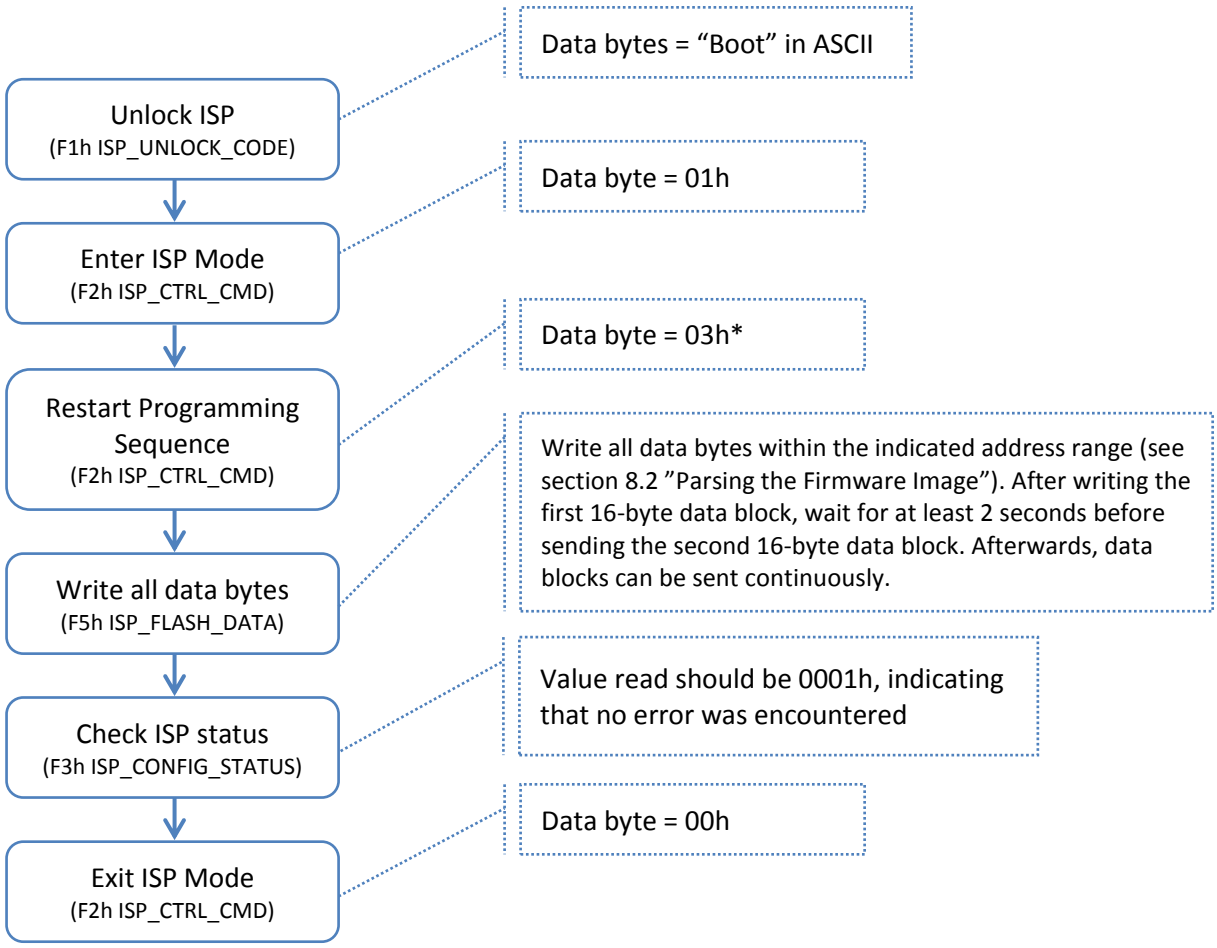
Record Type	Byte Count	Address	Data Words	Checksum
S3	11	00000500	54E1800554E1800554E2E430	2B

The number of data bytes allocated for the address varies depending on record type.

Record Type	Address Byte Count
S1	2
S2	3
S3	4

For more detailed reference about S-record: http://en.wikipedia.org/wiki/SREC_(file_format)

8.3. Firmware Update Process



In any case that the firmware update process fails (e.g. due to loss of power, communication error, etc.) the PSU will stay in ISP mode. The process must be reinitiated by going back to the Restart Programming Sequence step, and then continuing on to the next steps until Exit ISP Mode. After successful programming, the PSU will start up normally again.

9. FRU DATA

FRU data storage and retrieval is performed using PMBus USER_DATA_00 command. The FRU data size is 256 bytes. However, only a maximum of 16 bytes can be written or read in a single transaction.

To be able to access the FRU data, the following method is to be used:

1) First, indicate the starting location from which data access will be performed.
2) Then, indicate the number of bytes to be accessed consecutively from that point.
3) Finally, write to or read from the memory locations indicated.

The starting location in the array is indicated by a “Destination Byte Offset” byte for write accesses, and by a “Source Byte Offset” byte for read accesses. This byte offset can range from 0 to 255. The number of bytes to be accessed is indicated by a “Byte Count” byte. Its value can range from 1 to 16.

When doing a write transaction, if the Destination Byte Offset and Byte Count are greater than the range defined above, a CML error shall be triggered indicating an “Invalid or Unsupported Data Received” status.

Details on the write and read access protocols can be found on the succeeding sections.

9.1. Write Protocol

Writing to the User Data memory is performed using the block write protocol, as shown in the figure below:

S	Slave Addr / W	A	USER_DATA_00 Command Code	A	Byte Count = N+1, where 1 <= N <= 16	A	Destination Byte Offset	A

…

User Data Byte 1	A	User Data Byte 2	A	…	User Data Byte N-1	A	User Data Byte N	A	PEC	A	P

Starting from the location in User Data memory that the Destination Byte Offset points to, User Data Bytes 1 through N are written sequentially. Up to 16 bytes at a time can be written into the User Data memory. Byte Count is N+1 because one of the bytes in the transaction is the Destination Byte Offset.

9.2. Read Protocol

Reading from the User Data memory is performed using the block write-block read process call protocol, as shown in the figure below:

S	Slave Addr / W	A	USER_DATA_00 Command Code	A	Byte Count = 1	A	Source Byte Offset	A

…

Sr	Slave Addr / Rd	A	Byte Count = N, where 1 <= N <= 16	A	User Data Byte 1	A

…

User Data Byte 2	A	…	User Data Byte N-1	A	User Data Byte N	A	PEC	N	P

Starting from the location in User Data memory that the Source Byte Offset points to, User Data Bytes 1 through N are read sequentially. Up to 16 bytes at a time can be read from the User Data memory.

9.3. FRU Data Definition Table

For the FRU data, please refer to the following variant specific FRU Specs:

Variant	iPRO Part Number
DS2000SPE-3	970-012312-0000

10. PMBUS COMMANDS

10.1. Commands List Summary

This section summarizes all PMBus command codes that are supported.

Command Code	Command Name	Transaction Type	# of Data Bytes	Data Format	Write Protection	Additional Information
00h	PAGE	Read Byte	1	Hex	Basic	Default: 00h
01h	OPERATION	Read/Write Byte	1	Bitmapped	Basic	Default: 80h Valid input: 80h, 40h
02h	ON_OFF_CONFIG	Read Byte	1	Bitmapped	N/A	Default: 1Ch
03h	CLEAR_FAULTS	Send Byte	0	N/A	Basic	N/A
10h	WRITE_PROTECT	Read/Write Byte	1	Bitmapped	None	Default: 80h (write protect)
19h	CAPABILITY	Read Byte	1	Bitmapped	N/A	Default: 90h
1Ah	QUERY	Block Write – Block Read Process Call	1/1	Bitmapped	N/A	Varies
1Bh	SMBALERT_MASK	Write Word (Write) Block Write – Block Read Process Call and Write Word (Read)	2 (Write) 1/1 (Read)	Bitmapped	Basic	Default Mask: STATUS_VOUT - 0x6B STATUS_IOUT - 0x7F STATUS_INPUT - 0x6F STATUS_TEMP - 0x7F STATUS_CML - 0xFF STATUS_OTHER - 0xFF STATUS_FANS_1_2 - 0x3F
20h	VOUT_MODE	Read Byte	1	Bitmapped	N/A	Default: 17h
21h	VOUT_COMMAND	Read/Write Word	2	Linear (VOUT)	Basic	Default: 12.2V Valid Range: 11.6 – 12.8 V

Command Code	Command Name	Transaction Type	# of Data Bytes	Data Format	Write Protection	Additional Information
24h	VOUT_MAX	Read Word	2	Linear (VOUT)	N/A	Default: 12.8V
30h	COEFFICIENTS	Block Write – Block Read Process Call	2/5	Hex	N/A	m = 1, b = 0, R = 0
31h	POUT_MAX	Read Word	2	Linear	N/A	Default: 2000W
35h	VIN_ON	Read Word	2	Linear	N/A	Default: 88Vac
36h	VIN_OFF	Read Word	2	Linear	N/A	Default: 80Vac
3Ah	FAN_CONFIG_1_2	Read Byte	1	Bitmapped	N/A	Default: 90h
3Bh	FAN_COMMAND_1	Read/Write Word	2	Linear	Basic	Default: 0% Valid Range: 0 – 100%
40h	VOUT_OV_FAULT_LIMIT	Read/Write Word	2	Linear (VOUT)	User Configuration	Default: 14.5V Valid Range: 13.5 – 14.5 V
41h	VOUT_OV_FAULT_RESPONSE	Read Byte	1	Bitmapped	N/A	Default: 80h
42h	VOUT_OV_WARN_LIMIT	Read Word	2	Linear (VOUT)	N/A	Same as VOUT_OV_FAULT_LIMIT
43h	VOUT_UV_WARN_LIMIT	Read Word	2	Linear (VOUT)	N/A	Same as VOUT_UV_FAULT_LIMIT
44h	VOUT_UV_FAULT_LIMIT	Read/Write Word	2	Linear (VOUT)	User Configuration	Default: 10.25V Valid Range: 10.0 – 10.5 V
45h	VOUT_UV_FAULT_RESPONSE	Read Byte	1	Bitmapped	N/A	Default: 80h
46h	IOUT_OC_FAULT_LIMIT	Read Word	2	Linear	N/A	Default: 195A
47h	IOUT_OC_FAULT_RESPONSE	Read Byte	1	Bitmapped	N/A	Default: C0h
4Ah	IOUT_OC_WARN_LIMIT	Read/Write Word	2	Linear	N/A	Default: 175A Valid Range: 175 – 213 A
4Fh	OT_FAULT_LIMIT	Read Word	2	Linear	N/A	Default: 123 deg C
50h	OT_FAULT_RESPONSE	Read Byte	1	Bitmapped	N/A	Default: 78h

Command Code	Command Name	Transaction Type	# of Data Bytes	Data Format	Write Protection	Additional Information
51h	OT_WARN_LIMIT	Read Word	2	Linear	N/A	Default: 117deg C
56h	VIN_OV_FAULT_RESPONSE	Read Byte	1	Bitmapped	N/A	Default: 00h
57h	VIN_OV_WARN_LIMIT	Read Word	2	Linear	N/A	Default: 275Vac
58h	VIN_UV_WARN_LIMIT	Read Word	2	Linear	N/A	Default HL: 178 Vac Default LL: 88 Vac
59h	VIN_UV_FAULT_LIMIT	Read Word	2	Linear	N/A	Default HL: 172 Vac Default LL: 80 Vac
5Ah	VIN_UV_FAULT_RESPONSE	Read Byte	1	Bitmapped	N/A	Default: F8h
5Eh	POWER_GOOD_ON	Read Word	2	Linear (VOUT)	N/A	Default: 11.6V
5Fh	POWER_GOOD_OFF	Read Word	2	Linear (VOUT)	N/A	Default: 10.9V
60h	TON_DELAY	Read Word	2	Linear	N/A	Default: 100 ms
61h	TON_RISE	Read Word	2	Linear	N/A	Default: 100 ms
62h	TON_MAX_FAULT_LIMIT	Read Word	2	Linear	N/A	Default: 2.3S
63h	TON_MAX_FAULT_RESPONSE	Read Byte	1	Bitmapped	N/A	Default: 80h
64h	TOFF_DELAY	Read Word	2	Linear	N/A	Default: 2ms
6Ah	POUT_OP_WARN_LIMIT	Read Word	2	Linear	N/A	Default: 2100W
78h	STATUS_BYTE	Read Byte	1	Bitmapped	N/A	Default: 00h
79h	STATUS_WORD	Read Word	2	Bitmapped	N/A	Default: 0000h
7Ah	STATUS_VOUT	Read/Write Byte	1	Bitmapped	Basic	Default: 00h
7Bh	STATUS_IOUT	Read/Write Byte	1	Bitmapped	Basic	Default: 00h
7Ch	STATUS_INPUT	Read/Write Byte	1	Bitmapped	Basic	Default: 00h
7Dh	STATUS_TEMPERATURE	Read/Write Byte	1	Bitmapped	Basic	Default: 00h
7Eh	STATUS_CML	Read/Write Byte	1	Bitmapped	Basic	Default: 00h
81h	STATUS_FANS_1_2	Read/Write Byte	1	Bitmapped	Basic	Default: 00h

Command Code	Command Name	Transaction Type	# of Data Bytes	Data Format	Write Protection	Additional Information
86h	READ_EIN	Block Read	6	Direct	N/A	Varies
87h	READ_EOUT	Block Read	6	Direct	N/A	Varies
88h	READ_VIN	Read Word	2	Linear	N/A	Varies
89h	READ_IIN	Read Word	2	Linear	N/A	Varies
8Bh	READ_VOUT	Read Word	2	Linear (VOUT)	N/A	Varies
8Ch	READ_IOUT	Read Word	2	Linear	N/A	Varies
8Dh	READ_TEMPERATURE_1	Read Word	2	Linear	N/A	Pri Hotspot Default: 0 deg C if Primary is off
8Eh	READ_TEMPERATURE_2	Read Word	2	Linear	N/A	Sec Hotspot Default: 0 deg C if Primary is off
8Fh	READ_TEMPERATURE_3	Read Word	2	Linear	N/A	Secondary Ambient Default: 0 deg C if Primary is off
90h	READ_FAN_SPEED_1	Read Word	2	Linear	N/A	Varies
96h	READ_POUT	Read Word	2	Linear	N/A	Varies
97h	READ_PIN	Read Word	2	Linear	N/A	Varies
98h	PMBUS_REVISION	Read Byte	1	Bitmapped	N/A	Default: 22h
99h	MFR_ID	Block Read	Varies	ASCII	N/A	Default: "ARTESYN"
9Ah	MFR_MODEL	Block Read	Varies	ASCII	N/A	Default: "DS2000SPE-3"
9Bh	MFR_REVISION	Block Read	Varies	ASCII	N/A	Default: Varies
9Ch	MFR_LOCATION	Block Read	Varies	ASCII	N/A	Default: Varies

Command Code	Command Name	Transaction Type	# of Data Bytes	Data Format	Write Protection	Additional Information
9Dh	MFR_DATE	Block Read	Varies	ASCII	N/A	Default: Varies
9Eh	MFR_SERIAL	Block Read	Varies	ASCII	N/A	Default: Varies
A0h	MFR_VIN_MIN	Read Word	2	Linear	N/A	Default: 90 Vac
A1h	MFR_VIN_MAX	Read Word	2	Linear	N/A	Default: 264 Vac
A2h	MFR_IIN_MAX	Read Word	2	Linear	N/A	Default: 12.80 A
A3h	MFR_PIN_MAX	Read Word	2	Linear	N/A	Default LL: 1150 W Default HL: 2300 W
A4h	MFR_VOUT_MIN	Read Word	2	Linear (VOUT)	N/A	Default: 11.6V
A5h	MFR_VOUT_MAX	Read Word	2	Linear (VOUT)	N/A	Default: 12.8V
A6h	MFR_IOUT_MAX	Read Word	2	Linear	N/A	Default: 164 A
A7h	MFR_POUT_MAX	Read Word	2	Linear	N/A	Default: 2000 W
A8h	MFR_TAMBIENT_MAX	Read Word	2	Linear	N/A	Default: 55 deg C
A9h	MFR_TAMBIENT_MIN	Read Word	2	Linear	N/A	Default: 0 deg C
AAh	MFR_EFFICIENCY_LL	Block Read	14	Linear	N/A	Default: 115,200,88,500, 92,1000,89
ABh	MFR_EFFICIENCY_HL	Block Read	14	Linear	N/A	Default: 230,400,90,1000,94,2000,91
B0h	USER_DATA_00	Block Write (Write) Block Write – Block Read Process Call (Read)	Varies	Hex	Factory Configuration	N/A

Command Code	Command Name	Transaction Type	# of Data Bytes	Data Format	Write Protection	Additional Information
E0h	FW_PRI_VERSION	Block Read	8	ASCII	N/A	Varies
E1h	FW_SEC_VERSION	Block Read	8	ASCII	N/A	Varies
F1h	ISP_UNLOCK_CODE	Block Read/Write	4	ASCII	Basic	00h,00h,00h,00h
F2h	ISP_CTRL_CMD	Read/Write Byte	1	Bitmapped	Basic	N/A
F3h	ISP_CONFIG_STATUS	Read Word	2	Bitmapped	N/A	Varies
F5h	ISP_FLASH_DATA	Block Read/Write	16	Hex	ISP Mode	Varies

10.2. Reporting Accuracy

REPORTING FUNCTION	COMMAND CODE	COMMAND NAME	ACCURACY RANGE	
			5% to 20% load	20% to 100% load
Input Voltage	88h	READ_VIN	$\pm$ 5%	$\pm$ 5%
Input Current	89h	READ_IIN	$\pm$ $TBDA$ fixed error	$\pm$ 5%
Input Power	97h	READ_PIN	$\pm$ 5% ($\pm$ 5 W fixed error < 100W)	$\pm$ 5%
Output Voltage	8Bh	READ_VOUT	$\pm$ 5%	$\pm$ 2%
Output Current	8Ch	READ_IOUT	$\pm$ 10% ($\pm$ 0.8 A for < 10% load)	$\pm$ 10%
Output Power	96h	READ_POUT	$\pm$ 10%	$\pm$ 10%
Temperature	8Dh	READ_TEMPERATURE_1	$\pm$ 5 $degC$	$\pm$ 5 $degC$
	8Eh	READ_TEMPERATURE_2		
	8Fh	READ_TEMPERATURE_3		
Energy Input	86h	READ_EIN	$\pm$ 15% (from 10% - 20% load)	$\pm$ 5%
Fan Speed	90h	READ_FAN SPEED_1	$\pm$ 250 RPM	$\pm$ 250 RPM